A Fast Digital Predistortion Algorithm for Radio-Frequency Power Amplifier Linearization With Loop Delay Compensation

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***Abstract*—An adaptive, digital, baseband predistortion (PD) algorithm that compensates for the memoryless nonlinearities of radio-frequency (RF) power amplifiers (PAs) for wireless systems using non-constant-envelop modulation schemes is presented. Compared with the conventional, complex-gain predistorters based on lookup tables (LUTs), the proposed direct-learning, multilevel lookup table (ML-LUT) approach assisted by a hardware-efficient loop delay compensation scheme achieves a significant reduction in convergence time and an improvement in linearization accuracy in the presence of an unknown loopback delay. The experimental results in an FPGA prototyping platform show that the fast adaptation speed enables the predistorter to track time-varying PA nonlinearities as fast as in the tens of kilohertz range, constituting a potential solution for highly efficient PAs in mobile handsets.**

***Index Terms*—Baseband, digital predistortion, lookup table, loop delay compensation.**

I. Introduction

BASEBAND digital predistortion (PD or DPD) is a widely used linearity- and efficiency-enhancement technique for RF power amplifiers (PAs). A typical radio frequency (RF) transmitter with baseband PD is shown in Fig. 1, where an adaptive digital predistorter is employed to preprocess the baseband signal to cancel out the nonlinearities of the PA, thereby yielding an overall linear transfer function. Compared with alternative techniques, PD has certain advantages e.g., it can treat signals of much wider bandwidth than Cartesian feedback schemes [1], and is more economical than feed-forward compensation methods [2]. In addition, a digital approach is also much more amenable to fabrication technology scaling than its analog counterparts. As memory effects are often negligible in mobile applications [3], the dominant memoryless PA nonlinearities are usually modeled as the AM-AM and AM-PM distortions [4], which can be expressed as follows:

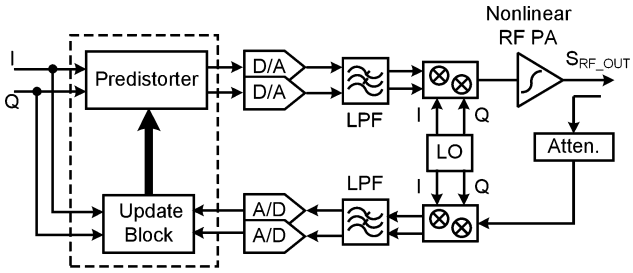

Fig. 1. System block diagram of an RF PA linearized by adaptive digital predistortion. The lower signal path facilitates the feedback.

$$v_{pa}(t) = F_{pa}\{r(t)\}\, e^{j[\varphi(t)+G_{pa}\{r(t)\}]} \tag{1}$$

where $v_{\rm in}(t) = r(t)e^{j\varphi(t)}$ is the complex baseband input signal, $v_{pa}(t)$ is the complex envelope of the PA's output, and $F_{pa}\{\bullet\}$ and $G_{pa}\{\bullet\}$ are the AM-AM and AM-PM distortion functions, respectively, both of which are determined solely by the amplitude of the PA's input signal. Typical such distortion curves are shown in Fig. 2 for a 5-GHz, two-stage, 0.13-μm CMOS, Class-B PA for 802.11x OFDM applications [5]. Since the cascaded transfer characteristic of the PA and the predistorter is linear, the PD transfer function must ideally satisfy the following equations:

$$F_{\rm total}\{r(t)\} = F_{pa}\{F_{pd}\{r(t)\}\} = G_0 r(t) \tag{2}$$

$$G_{\rm total}\{r(t)\} = G_{pa}\{F_{pd}\{r(t)\}\} + G_{pd}\{r(t)\} = 0 \tag{3}$$

where $F_{pd}\{\bullet\}$ and $G_{pd}\{\bullet\}$ are the AM-AM and AM-PM PD functions, respectively, $F_{\rm total}\{\bullet\}$ and $G_{\rm total}\{\bullet\}$ are the AM-AM and AM-PM responses of the overall transmitter, respectively, and G_0 is the voltage gain of the transmitter, which is unity in a normalized sense. In this paper, the range of normalization is $[-1, 1]$.

According to the architecture and adaptation strategy of a DPD transmitter, prior works on DPD can be cast into the following categories: the polynomial method [6], lookup table method [7]–[9], neural network method [10], and cumulative density function (CDF) method [11], [12]. Among various PD techniques, the LUT-based scheme, in which the inverse function of the PA is stored in a memory, is most attractive due to its compensation accuracy and simplicity. Compared with the polynomial-based PD, an LUT can accurately fit to

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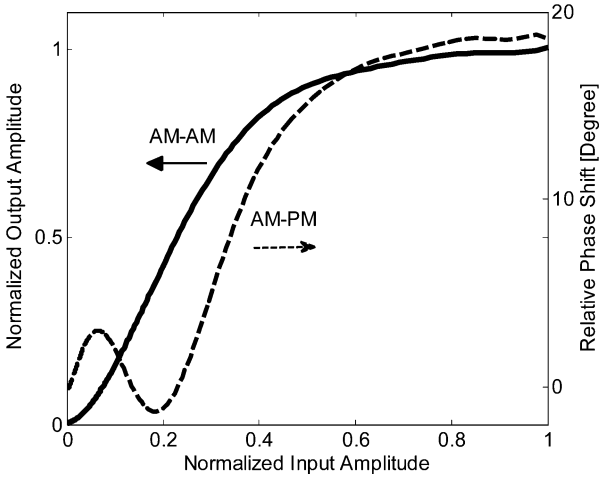

Fig. 2. Typical AM-AM and AM-PM distortion curves of a Class-B, CMOS RF PA.

nearly any nonlinear curve given enough memory. The first LUT-based predistorter was developed by Nagata [7] with a two-dimensional memory. A complex-gain-based LUT PD was proposed by Cavers [8] to reduce the memory required and to improve the adaptation speed. Nonetheless, the conventional LUT PD approaches suffer from a severe performance tradeoff between the adaptation speed and compensation accuracy, since the convergence time is linearly proportional to LUT size (i.e., accuracy) [13]. Specifically, in a multicarrier quadrature amplitude modulation (QAM) system, the amplitude of the input signal is nearly Rayleigh-distributed [14]; and as a result, the entries of the LUT will not be accessed uniformly—those residing in the lower middle (amplitudes) are frequently updated and thus converge quickly, while others (particularly the high end) see rare visits, which significantly impedes the adaptation performance of the transmitter.

Although the deployment of LUT-based PD technology in base-stations is prevalent and several commercial products have been offered off the shelf [15]–[18], very few have been incorporated into handset devices. For the base-station case, the PD linearizers are usually full-featured, hardware complex, power hungry, and suitable for compensating various imperfections of high-power RF transmitters including memory effect and I/Q imbalance [15], [16]. However, most of these features are not needed in mobiles; and the handset predistorters have their own unique features—the high mobility of the handsets dictates that the predistorters perform fast adaptation to track the time-varying characteristics of the PA distortion. In addition, the delay of the RF feedback loop in Fig. 1, especially the fractional part (in contrast to the integer sample periods) is another essential parameter affecting the PD performance [19], which unfortunately varies from device to device and is also a function of the ambient environment. It is therefore necessary to estimate this loopback delay and compensate for it. Meanwhile, low hardware complexity and power consumption are also critical. All these requirements present keen challenges for the PD design in handset applications.

In the past, quite a few techniques have been developed to expedite the initial convergence of the LUT PD. In [20], a joint polynomial and LUT architecture was proposed, in which polynomial coefficients are updated first, and the adaptation is switched to LUT subsequently for an accurate compensation. In [21], a broadcasting technique with training signals was introduced. At the beginning of the training mode, the algorithm updates blocks of memory cells simultaneously instead of single cells, and then gradually decrements the block size to reach steady state. In [22], various quantization levels were adopted. A large quantization level is used to update for only a limited number of amplitudes at the beginning; while after a certain number of iterations, interpolation is employed to estimate all contents in the LUT, followed by updating with a fine quantization level. In [23], a linear approximation was performed using the previously modified values at the two neighboring cells below and above the current address to smooth the LUT contents. Lastly, a non-iterative adaptive predistorter was presented in [24], where an indirect learning strategy and a ramp training signal were employed in the initialization phase. In summary, all the above techniques are effective in expediting the initial adaptation of the predistorter; however, the initial convergence time bears little significance when it comes to the tracking performance in mobiles, largely due to, as mentioned before, their highly heterogeneous and dynamic operating environment (in contrast to that of the base-stations).

On the other hand, for the loop delay estimation and compensation, the algorithmic complexity and compensation accuracy are the key issues. Some previous works are summarized as follows. The loop delay estimation algorithm presented in [7] is known to lack accuracy; the scheme in [25] using a fast Fourier transform (FFT) involves intensive and time-consuming computations; the technique proposed in [26] requires a high oversampling ratio ($64\times$) to achieve the desired accuracy; the method involving a ramp training sequence proposed in [19] is sufficiently accurate but not adaptive; lastly, the cross-correlation, adaptive estimator in [27] requires a large number of multiplications, and hence is costly for hardware implementation.

Targeting mobile applications, this paper proposes a multilevel LUT (ML-LUT) PD approach for fast adaptation in conjunction with a hardware-efficient, adaptive, loop delay estimation algorithm, in which the use of multipliers is minimized. For fast prototyping and performance evaluation of the proposed algorithm, an experimental platform was built in an FPGA (Altera Stratix II) using fixed-point arithmetic. Experimental results from the emulation demonstrate that the proposed PD algorithm not only converges faster than the conventional LUT-based PD schemes, it also exhibits a much lower steady-state mean-square error (MSE), as compared to the polynomial-based PD approaches.

The rest of the paper is organized as follows. Section II provides a detailed description of the proposed algorithm; Section III illustrates several experimental results from the FPGA emulation; and Section IV concludes this paper.

II. Proposed Predistortion Approach

The proposed baseband adaptive digital predistorter uses a complex-gain-based scheme, in which the compensation factor

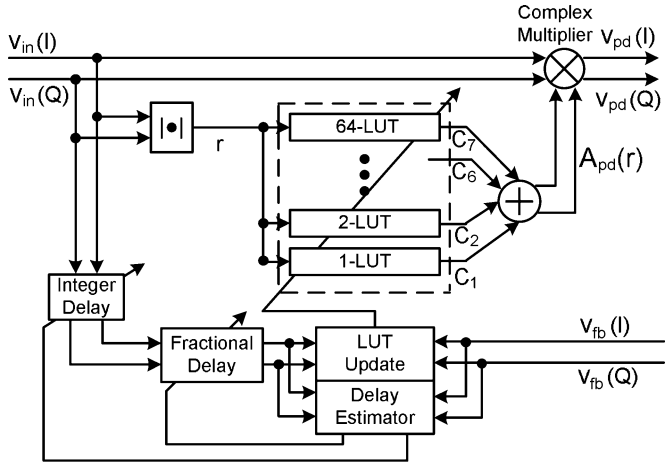

Fig. 3. Functional block diagram of the proposed ML-LUT adaptive digital predistorter ($N = 7$) for RF PA linearization.

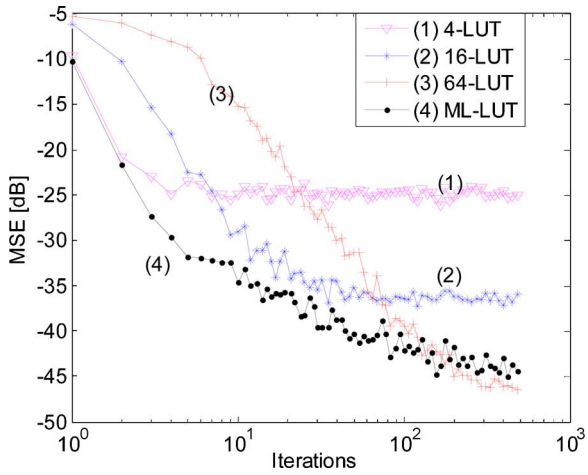

Fig. 4. Learning curves of ML-LUT ($N = 7$, $\mu = 1/32$ for each table or $\mu_{eq} = 7/32$) and conventional LUTs ($\mu = 7/32$) with uniformly distributed random input signal.

is expressed as the complex gain $A_{pd}\{r(n)\}$ in a Cartesian representation

$$v_{pd}(n) = v_{\text{in}}(n) A_{pd}\{r(n)\} \tag{4}$$

where

$$\begin{aligned} \text{Re}\left(A_{pd}\{r(n)\}\right) &= \frac{F_{pd}\{r(n)\}}{r(n)} \cos\left(G_{pd}\{r(n)\}\right) \\ \text{Im}\left(A_{pd}\{r(n)\}\right) &= \frac{F_{pd}\{r(n)\}}{r(n)} \sin\left(G_{pd}\{r(n)\}\right). \end{aligned} \tag{5}$$

Here, a discrete-time notation is used. The block diagram of the proposed approach is shown in Fig. 3, which consists of two parts: a multilevel LUT-based nonlinear compensator and a loop delay estimator and adjustor, both of which are adaptive.

A. Multilevel LUT-Based Predistorter

To eliminate the tradeoff between the adaptation speed and compensation accuracy in conventional LUT-based PD approaches (manifested by the first three curves in Fig. 4), we introduce a multilevel LUT (ML-LUT) scheme, which has built-in interdependence between the LUT cells. An ML-LUT is constructed by N parallel LUTs with geometrically incrementing sizes from 1 to 2^{N-1} (a total of $2^N - 1$ memory cells). The overall PD function is formed by summing the outputs of the N LUTs

$$A_{pd}\{r(n)\} = \sum_{k=0}^{N-1} C_k\left\{\left\lfloor 2^k r(n)\right\rfloor\right\} \tag{6}$$

where $A_{pd}\{r(n)\}$ is the complex PD multiplicand, and $C_k\{\lfloor 2^k r(n)\rfloor\}$ denotes the content of the k^{th} LUT addressed by the quantized/normalized input amplitude $\lfloor 2^k r(n)\rfloor$. The amplitude-addressing method is chosen for its better tradeoff between complexity and accuracy, in contrast to other methods [28]. In Fig. 3, a 7-level ML-LUT consisting of 7 tables with sizes of 1, 2, 4, 8, 16, 32, and 64, respectively, and a total of 127 memory cells is shown as an example. Each table is trained by a least mean-square (LMS) algorithm. For the k^{th} table (k ranges from 0 to $N-1$), the iterative update equation is

$$C_k\{\bullet\}_{n+1} = C_k\{\bullet\}_n + \mu v_{\text{in}}^*(n)\left[v_{\text{in}}(n) - v_{fb}(n)\right] \tag{7}$$

where $v_{\text{in}}^*(n)$ is the complex conjugate of the input signal, $v_{fb}(n)$ is the feedback signal, and μ is the update step size for each table. Substituting C_k in (6) with (7), we have

$$A_{pd}\{\bullet\}_{n+1} = A_{pd}\{\bullet\}_n + N\mu v_{\text{in}}^*(n)\left[v_{\text{in}}(n) - v_{fb}(n)\right] \tag{8}$$

i.e., the equivalent step size for the ML-LUT is $\mu_{eq} = N\mu$.

The built-in interdependence between the multi-tables enables us to exploit the speed of a small table and the accuracy of a large table simultaneously in the proposed scheme. In other words, with ML-LUT, the compensation accuracy is determined by the fine tables, and the coarse tables help to expedite the convergence. Fig. 4 shows the comparison of the learning curves of a 7-level ML-LUT and three conventional LUTs with equivalent step sizes and identical word lengths. Compared with the conventional 64-LUT, the 7-level ML-LUT requires double the memory size, while reducing the convergence time by approximately 9× (the convergence time is defined as the number of iterations before the MSE reaches −30 dB). The overhead in memory size is nearly negligible when implemented in deeply scaled CMOS processes.

The comparison of the steady-state mean-square error (MSE) and convergence time between the N-level ML-LUT and conventional 2^{N-1}-LUT is shown in Fig. 5, where the x-axis corresponds to the size of the conventional LUT. For the conventional LUTs, the convergence time increases linearly as a function of the LUT size, while for ML-LUT, the convergence time remains nearly constant. Meanwhile, the MSE of the N-level ML-LUT is slightly (0.5 dB) larger than that of the conventional 2^{N-1}-LUT. In fact, the slight MSE degradation is mainly attributable to a phenomenon termed *stalling* [29] due to the finite

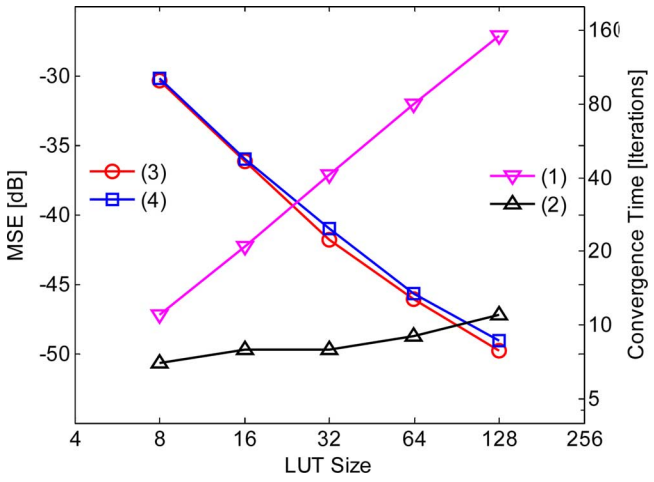

Fig. 5. Performance comparison between conventional LUT and ML-LUT with uniformly distributed random input signal: (1) convergence time for LUT, (2) convergence time for ML-LUT, (3) MSE for LUT, and (4) MSE for ML-LUT.

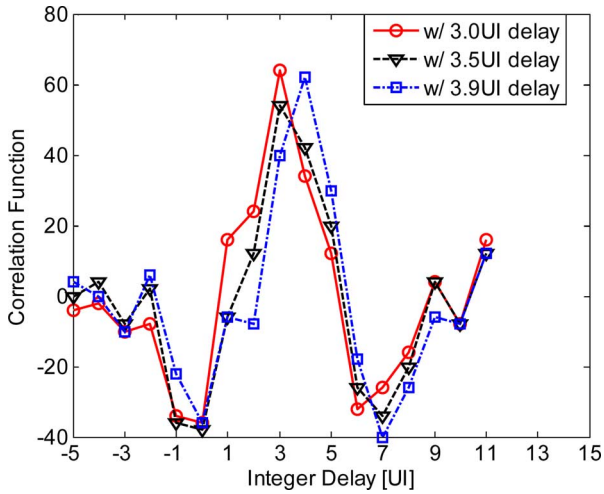

Fig. 6. Evaluation of the amplitude-difference correlation function.

word-length effect—the coefficient update stops when the following condition holds

$$|\mu v^*(n)e(n)| < 1\ LSB. \tag{9}$$

Note that the step size for each table in the N-level ML-LUT is only $1/N$ of that in the 2^{N-1}-LUT; and stalling is more significant in the ML-LUT case when the word lengths are the same. Further experiments reveal that, with larger step sizes, the MSE difference between the two methods becomes increasingly negligible.

A similar exploitation of the features of coarse and fine tables has been reported in the broadcasting technique [21]. However, there the characteristic is temporal and only exists in the initialization phase. The ML-LUT method proposed here retains the interdependence between multi-tables in a hardwired configuration, thereby enabling the scheme to track time-varying PA characteristics at all times without losing compensation accuracy.

B. Integer Loop Delay Estimation

The loop delay compensation is accomplished in two steps. In the first step, an integer delay is estimated from the amplitude-difference correlation function of the input signal and the feedback signal:

$$R(m) = \sum_{i=1}^{M} D\left[v_{\text{in}}(i-m)\right] D\left[v_{fb}(i)\right] \tag{10}$$

where M is the sequence length to calculate the correlation, m is the estimated integer delay, and the amplitude-difference function $D(\bullet)$ is defined as

$$D\left[v(n)\right] = sign\left[|v(n)| - |v(n-1)|\right]. \tag{11}$$

Note that the feedback signal is a severely distorted (stretched and rotated) version of the input signal initially. However, the AM-AM distortion curve is almost monotonic for the input signals below the saturation level, shown in Fig. 2, especially for OFDM signals, most of which are located far away from the saturation region. This fact guarantees that larger input amplitude always results in a larger feedback signal; thus, the polarity of the amplitude-difference between neighboring samples will be retained even with the PA's distortion, justifying the use of the amplitude-difference correlation to determine the integer loop delay. The delay m that maximizes the correlation function is the closest integer delay of the loop. Fig. 6 shows the amplitude-difference correlation function with $M = 64$ under various estimated delay m (horizontal axis), where the actual integer delay is set to 3 clock cycles or unit intervals (UIs) with a fractional delay of 0, 0.5 UI and 0.9 UI, respectively. For the case of 3.5-UI delay, the integer part is estimated to be 3 UIs and the residual fractional part is 0.5 UI; while for the case of 3.9-UI delay, the integer part is estimated to be 4 UIs and the residual part is -0.1 UI. Also note that the multiplication in (10) can be replaced by an XOR function, and (11) can be realized by a comparator. The architecture proposed here not only significantly simplifies the hardware implementation, but also enhances the estimation robustness over the PA's gross nonlinearity.

Fig. 7 illustrates the implementation of the integer delay estimator, which searches the delay m from 0 up to 7 UIs. When the peak of the correlation function is found, the *Delay Locked* signal is asserted, which stops the counter and subsequently outputs m. The decision threshold is set at $M/2$ to desensitize the algorithm to the effect of random noise.

C. Fractional Loop Delay Estimation and Compensation

The residual fractional loop delay (θ) is located in the range of (-UI, UI) after the integer delay has been corrected, and can be compensated by a 4-tap FIR interpolation filter with a modified Farrow structure [30]. The Farrow FIR filter that produces a positive delay is revised here to accommodate both the positive and negative fractional delays (shown in Fig. 8). In either case,

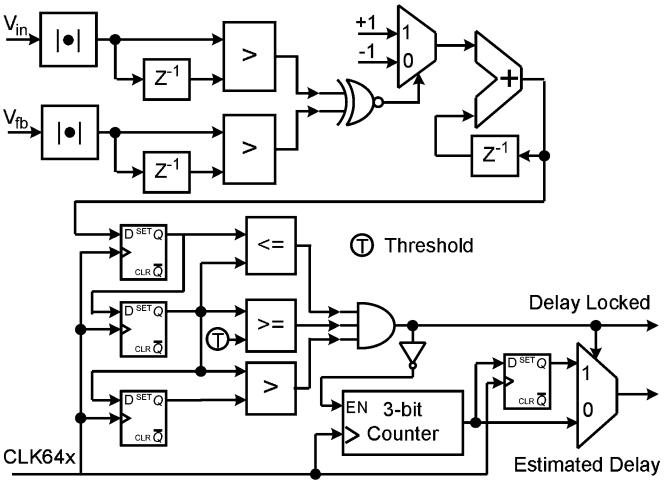

Fig. 7. Integer loop delay estimation module.

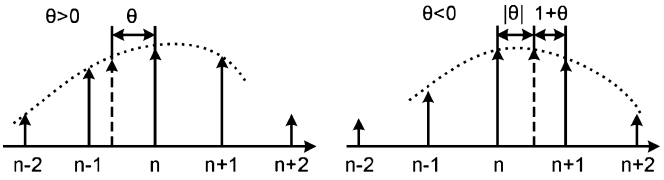

Fig. 8. Positive and negative fractional loop delays.

the nearest four neighboring samples are involved in estimating the delayed sample with the following interpolation functions:

$$y_{\text{in}}(n) = \begin{cases} \sum_{i=-2}^{1} a_i(\theta) x_{\text{in}}(n+i), & (\theta > 0) \\ \sum_{i=-2}^{1} a_i(1+\theta) x_{\text{in}}(n+1+i), & (\theta < 0) \end{cases} \tag{12}$$

where

$$\begin{aligned} a_1(\theta) &= \alpha\theta^2 - \alpha\theta \\ a_0(\theta) &= -\alpha\theta^2 + (\alpha - 1)\theta + 1 \\ a_{-1}(\theta) &= -\alpha\theta^2 + (\alpha + 1)\theta \\ a_{-2}(\theta) &= \alpha\theta^2 - \alpha\theta \end{aligned}$$

where $x_{\text{in}}(n)$ represents either the real or imaginary part of the complex input signal $v_{\text{in}}(n)$, and a similar formulation is applicable to $x_{fb}(n)$ and $v_{fb}(n)$. $y_{\text{in}}(n)$ is the delayed version of $x_{\text{in}}(n)$, and α is a design parameter between 0 and 1. When α is 0, the 4-tap filter degenerates to a linear interpolator. The interpolation is actually a weighted average of four neighboring samples, of which the nearest two are more important and carry larger weights.

To derive an iterative equation to estimate θ, let us first assume that the actual fractional loop delay is $\theta_0 > 0$. With the same interpolation functions, the delayed feedback signal can be expressed as

$$y_{fb}(n) = \sum_{i=-2}^{1} a_i(\theta_0) x_{fb}(n+i) \tag{13}$$

where $x_{fb}(n)$ and $y_{fb}(n)$ are the feedback sequence without and with fractional loop delay, respectively, and $x_{\text{in}}(n) \approx x_{fb}(n)$ holds with a linearized transmitter. Define

$$e(n) = y_{\text{in}}(n) - y_{fb}(n) \tag{14}$$

$$\begin{aligned} F_{-1} &= E\{x_{\text{in}}(n-1)e(n)\} \\ &\approx \sum_{i=-2}^{1} [a_i(\theta) - a_i(\theta_0)] \\ &\quad \times E\{x_{\text{in}}(n-1)x_{\text{in}}(n+i)\} \end{aligned} \tag{15}$$

$$\begin{aligned} F_0 &= E\{x_{\text{in}}(n)e(n)\} \\ &\approx \sum_{i=-2}^{1} [a_i(\theta) - a_i(\theta_0)] \\ &\quad \times E\{x_{\text{in}}(n)x_{\text{in}}(n+i)\} \end{aligned} \tag{16}$$

where $E\{\bullet\}$ is the expectation function. Also consider that $x_{\text{in}}(n)$ is a stationary sequence; hence

$$E\{x_{\text{in}}(n)x_{\text{in}}(n+i)\} = E\{x_{\text{in}}(n-i)x_{\text{in}}(n)\}. \tag{17}$$

In addition, note that

$$a_1(\theta) - a_{-2}(\theta) = 0, \quad a_{-1}(\theta) - a_0(\theta) = 2\theta - 1. \tag{18}$$

Utilizing (15)–(18), we have

$$\begin{aligned} F_0 - F_{-1} &= E\{[x_{\text{in}}(n) - x_{\text{in}}(n-1)]\, e(n)\} \\ &\approx \sum_{i=-2}^{1} [a_i(\theta) - a_i(\theta_0)] \\ &\quad \times E\{[x_{\text{in}}(n) - x_{\text{in}}(n-1)]\, x_{\text{in}}(n+i)\} \\ &= 2E\left\{x_{\text{in}}^2(n) - x_{\text{in}}(n-1)x_{\text{in}}(n)\right\}(\theta_0 - \theta). \end{aligned} \tag{19}$$

Define $p = 2E\{x_{\text{in}}^2(n) - x_{\text{in}}(n-1)x_{\text{in}}(n)\}$, and $p \geq 0$ holds almost surely in general. Thus, we can estimate the delay with the following iteration using a block LMS algorithm:

$$\begin{aligned} \theta_{m+1} &= \theta_m + \beta p(\theta_0 - \theta_m) \\ &= \theta_m + \beta E\{[x_{\text{in}}(n) - x_{\text{in}}(n-1)]\, e(n)\} \\ &= \theta_m + \frac{\beta}{L} \sum_{j=0}^{L-1} \{x_{\text{in}}(mL+j) - x_{\text{in}}(mL+j-1)\} \\ &\quad \times e(mL+j) \end{aligned} \tag{20}$$

where L is the LMS block length, and β is the step size and must satisfy the requirement $0 < \beta p < 2$ to guarantee stability. Furthermore, for convergence, the multiplicand $[x_{\text{in}}(n) - x_{\text{in}}(n-1)]$ can be replaced by a monotonic function of itself [31], e.g., its sign for the sake of simplicity, which is known as the Clipped-Data LMS algorithm [32].

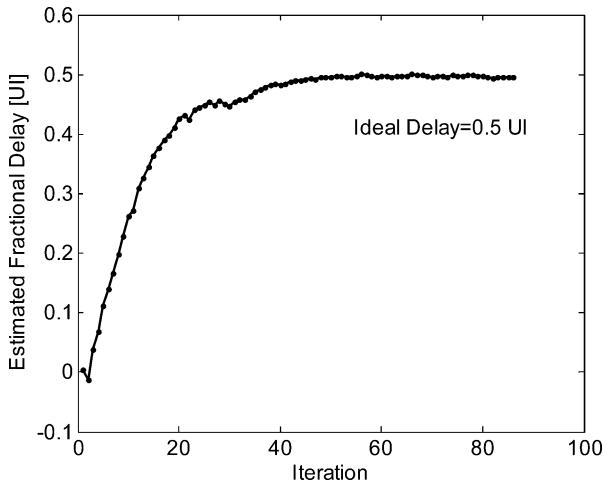

Fig. 9. Learning curve of the fractional loop delay estimation ($N = 32$, $\beta = 2$).

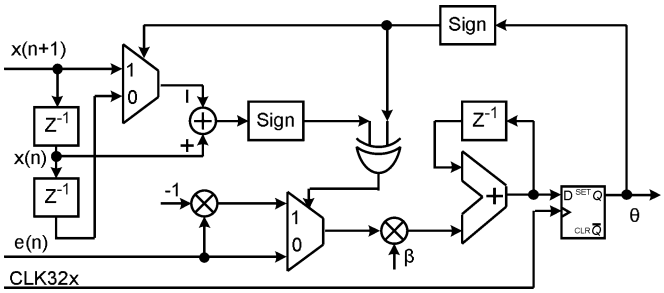

Fig. 10. Adaptive fractional loop delay estimation module.

Following the same procedure, we can obtain a similar iterative equation for the case of $\theta_0 < 0$. The overall fractional delay estimation is summarized as

$$\theta_{m+1}=\theta_m+\begin{cases}\frac{\beta}{L}\sum_{j=0}^{L-1} sign\left[x_{\rm in}(mL+j)\right. \\ \quad \left.-x_{\rm in}(mL+j-1)\right]e(mL+j) \quad (\theta_m>0) \\ -\frac{\beta}{L}\sum_{j=0}^{L-1} sign\left[x_{\rm in}(mL+j)\right. \\ \quad \left.-x_{\rm in}(mL+j+1)\right]e(mL+j) \quad (\theta_m<0).\end{cases} \tag{21}$$

Note that a larger block length will improve the stability of the algorithm, however at the cost of a slow convergence and a degraded tracking performance. Fig. 9 shows the learning curve with a block length of 32.

Fig. 10 shows the implementation of the fractional delay estimator with a block length of 32. Fig. 11 illustrates the revised 4-tap Farrow FIR filter, where the multiplexers are controlled by the sign from the fractional delay estimator. The parameter α is set to 0.25 for both hardware simplicity and interpolation accuracy in this work. Hence, there are only two real multipliers required for each of the I- and Q-channel.

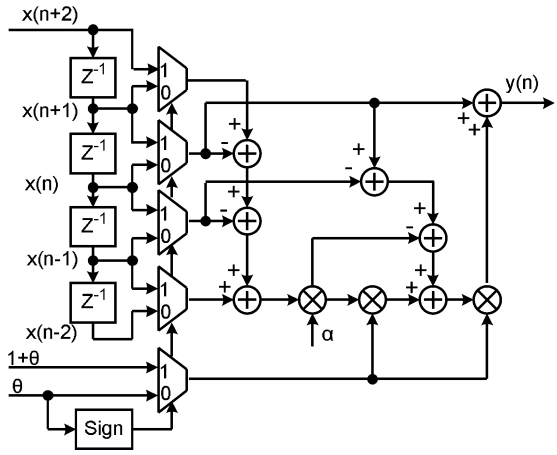

Fig. 11. Fractional loop delay compensation module.

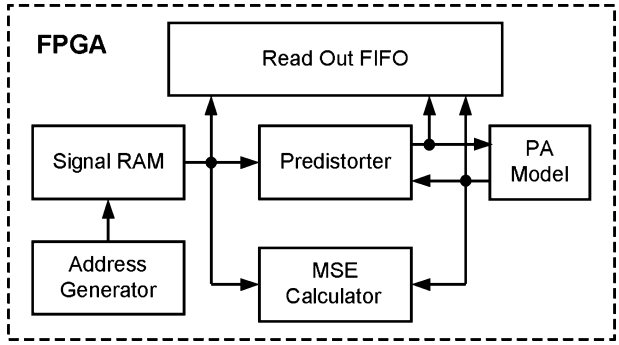

Fig. 12. Block diagram of the FPGA emulation platform.

TABLE I
HARDWARE COMPLEXITY OF VARIOUS PD TREATMENTS

	Multiplier	Adder	Memory
5th-order polynomial	36	18	0
64-LUT	8	8	64×28 bits
7-level ML-LUT	8	15	127×28 bits
Loop delay comp.	4	20	0

III. EXPERIMENTAL RESULTS

A. Emulation Platform

In order to evaluate the proposed ML-LUT scheme with loop delay compensation and to compare its performance with other PD approaches, a hardware emulation platform was constructed using an Altera Stratix II FPGA, which includes a 7-level ML-LUT PD with loop delay compensation, a conventional 64-LUT PD, and a 5th-order polynomial PD. Fig. 12 is the block diagram of the FPGA emulation platform, including a baseband signal generator, a PA model, an MSE calculator, a readout FIFO, and some control logics. Table I lists the hardware costs of the three PD approaches.

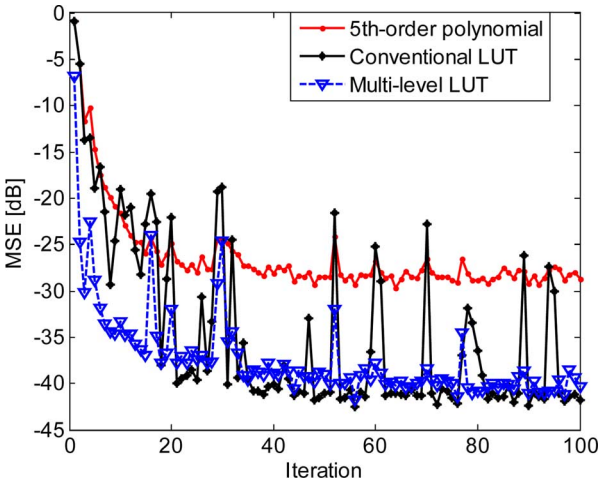

Fig. 13. Initial learning curves of the three PD algorithms.

In emulation, the AM-AM and AM-PM distortion curves in Fig. 2 extracted from a 5-GHz, class-B CMOS PA [5] were fit to two high-order polynomials

$$F_{pa}\{r(n)\} = \sum_{i=0}^{P} a_i r(n)^i, \quad G_{pa}\{r(n)\} = \sum_{i=0}^{Q} b_i r(n)^i \tag{22}$$

where $P = 7$ and $Q = 11$.

In the experiment, a 64-QAM OFDM signal was adopted as the baseband input signal, which consists of 64 subcarriers with a 20-MHz bandwidth, an 11-dB peak-to-average power ratio (PAPR), and a 0-dB peak back-off (PBO). A typical 4× oversampling, i.e., a sample rate of 80 MHz, was assumed with 10-bit DAC and ADC in the TX and RX, respectively. The predistorter is initialized as "transparent," i.e., the output equals the input at the beginning. The emulation runs at an actual clock frequency of 50 MHz. Some experimental results are discussed in detailss in this section.

B. Convergence

The learning curves of three adaptive predistorters, i.e., the fifth-order polynomial, 64-LUT, and 7-level ML-LUT, during initialization are shown in Fig. 13, where each iteration consists of 256 samples. The step sizes for the LUT methods are 7/32 as before, while the step size for the polynomial PD is set to 0.05, nearly the maximum value for an acceptable MSE in steady state. The emulation results indicate that the proposed ML-LUT scheme converges significantly faster than the conventional LUT PD and exhibits lower steady-state errors than the polynomial PD. In addition, the conventional LUT curve shows occasional large error spikes that are mainly attributable to the rarely updated LUT cells residing at the upper end. These spikes severely degrade the performance of the algorithm in the steady state. Note that this phenomenon largely disappears in the proposed ML-LUT approach.

TABLE II
MSE AND ACPR PERFORMANCE

	MSE	ACPR
PA output w/o PD	-1.72 dB	53.4 dB
5th-order polynomial	-32.4 dB	66.7 dB
64-LUT	-40.6 dB	72.4 dB
7-level ML-LUT	-40.4 dB	72.3 dB
Ideal PA	n/a	75.7 dB

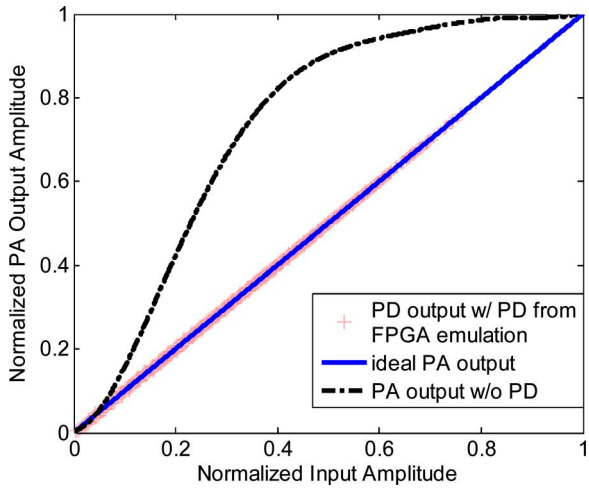

Fig. 14. AM-AM curves of the Class-B PA w/ and w/o ML-LUT PD.

C. Steady-State Performance

Table II summarizes the steady-state MSE and adjacent channel power ratio (ACPR) performance of the three PD algorithms upon training. It is apparent that the two LUT schemes exhibit comparable steady-state performance, and both are better than that of the polynomial approach. Fig. 14 shows the PA transfer curve with and without the ML-LUT PD. Note that the compensated curve is drawn with data from the actual emulation; hence, the data points of large amplitude are rare due to the 11-dB PAPR of the OFDM signal.

D. Tracking Performance

A simplified time-varying PA was modeled as follows:

$$F'_{pa}\{r(n)\} = F_{pa}\{r(n)\}\{1 + A_0 \sin(2\pi f t)\} \tag{23}$$

$$G'_{pa}\{r(n)\} = G_{pa}\{r(n)\} + B_0 \sin(2\pi f t) \tag{24}$$

where the PA's AM-AM and AM-PM responses are assumed to vary with time in a sinusoidal fashion—f denotes the variation frequency, A_0 is the peak AM-AM variation, which is set to 10%, and B_0 is the peak AM-PM variation, which is also set to 10% of the maximum phase shift around 20°.

Experimental results demonstrate that the MSE rises with the increase of f for all PD algorithms (Fig. 15). The proposed ML-LUT is most insensitive to fast variations—capable of

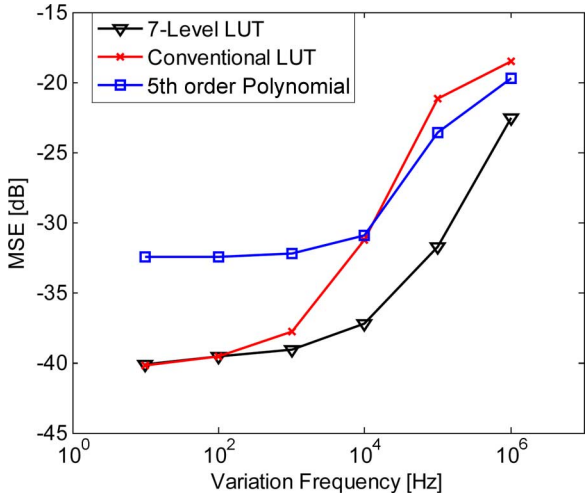

Fig. 15. Tracking performance of the three PD algorithms.

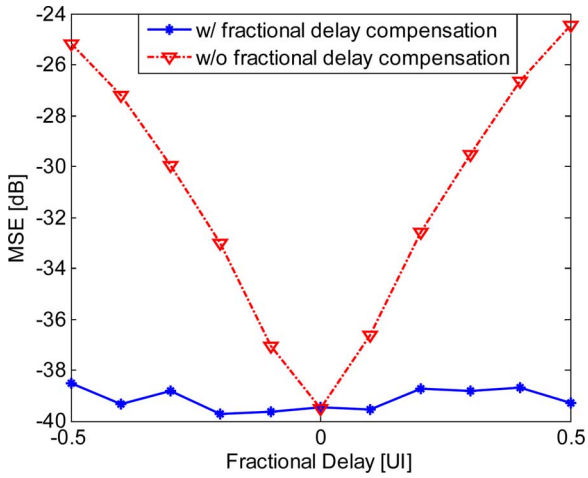

Fig. 16. Performance of fractional loop delay compensation.

tracking variations of tens of kilohertz; while the conventional LUT PD is the most sensitive algorithm. The ML-LUT technique therefore enhances the tracking capability of LUT-based PD approaches significantly.

E. Performance of Loop Delay Compensation

When a loop delay is present, the MSE performance with and without the proposed fractional loop delay correction is shown in Fig. 16. The MSE rises up dramatically with the increase of the fractional delay without compensation, and becomes quite insensitive to it with compensation. Since the fractional delay estimator is adaptive, the predistorter is capable of tracking any loop delay variation caused by the environment. Fig. 17 shows the output spectra of the PA with a 0.5-UI loop delay. The loop delay compensation improves the ACPR by 9.5 dB in this experiment.

F. Word Length (WL) and Step Size

Table III summarizes the impact of WL on the compensation accuracy of the ML-LUT PD. In this work, the inner WL was chosen to be 14 bits. In addition, the step sizes of the LMS algorithm were optimized based on emulations, with the results

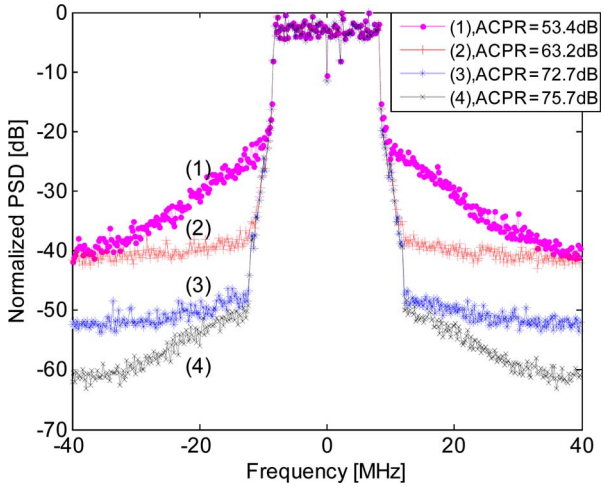

Fig. 17. PA output spectra with a 0.5-UI loop delay: (1) without PD, (2) with ML-LUT PD alone, (3) with ML-LUT PD and loop-delay compensation, and (4) with ideal PA.

TABLE III
WORD-LENGTH EFFECT ON MSE

WL [bits]	10	11	12	13	14	15
MSE [dB]	-29.8	-31.3	-33.3	-34.9	-39.1	-39.7

TABLE IV
STEP-SIZE EFFECT ON MSE

μ_{eq}/μ_0	1/8	1/4	1/2	1	2	4
MSE [dB]	-25.2	-31.3	-35.2	-40.4	-40.8	-24.4

shown in Table IV, in which the nominal step size μ_0 is set to 7/32 (1/32 for each table). Because of the finite WL effect, too small a step size will stop the adaptation due to stalling, while too large a step size will possibly destabilize the algorithm. The fixed-point results obtained from hardware emulation are bit-accurate, and can serve as the guidelines for a future ASIC implementation.

G. Quantization Effects of ADC and DAC

The accuracy of the PD compensation also suffers from the finite resolution of the data converters used in the TX and RX. Fig. 18 shows the MSE performance of the proposed ML-LUT with different ADC and DAC resolutions. It is revealed that the DAC resolution is more critical than the ADC—perhaps because the DAC outputs drive the PA directly, and the quantization noise passes through without attentuation, while the ADC outputs are used to update the LUT contents and the quantization noise effect is mitigated by the averaging (of the LMS loop). These observations are helpful for system-level designs, in which low resolution converters can be adopted for cost reduction.

IV. CONCLUSION

A ML-LUT-based, adaptive, digital, baseband predistortion architecture for RF power amplifier linearization is presented. The ML-LUT approach mitigates the primary drawback of the conventional, adaptive LUT techniques, i.e., the tradeoff

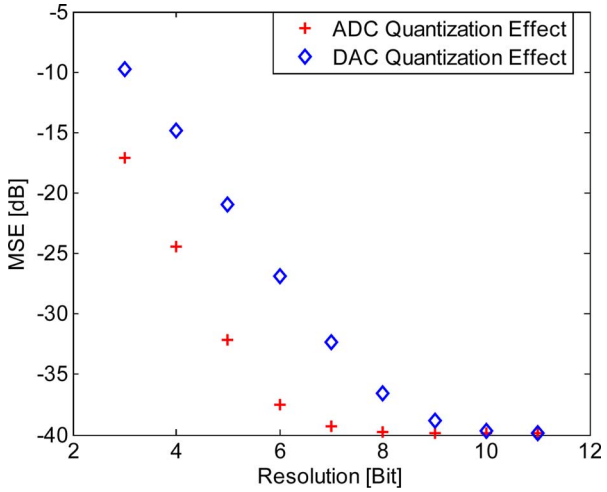

Fig. 18. Quantization effects of ADC and DAC.

between the compensation accuracy and adaptation speed. Compared with the conventional LUT and polynomial-based predistorters, the proposed algorithm significantly enhances the dynamic behavior of the treatment while preserving the inherent advantages of an LUT-based approach, including the hardware efficiency and high compensation accuracy. In addition, an adaptive loop delay estimation and compensation scheme is introduced, which assists the PD algorithm and can reduce MSE and improve ACPR significantly in the presence of an unknown loopback delay.

FPGA emulation demonstrates the advantages of our approach, i.e., tracking speed, high compensation accuracy, and hardware simplicity. The proposed technique provides a viable solution to the PA problem of future mobile terminals with simultaneous high power efficiency and linearity.

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REFERENCES

[1] J. L. Dawson and T. H. Lee, "Automatic phase alignment for a fully integrated Cartesian feedback power amplifier system," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2269–2279, Dec. 2003.
[2] C. Hsieh and S. Chan, "A feedforward S-Band MIC amplifier system," *IEEE J. Solid-State Circuits*, vol. SC-11, no. 2, pp. 271–278, Apr. 1976.
[3] J. Deng, P. S. Gudem, L. E. Larson, D. F. Kimball, and P. M. Asbeck, "A SiGe PA with dual dynamic bias control and memoryless digital predistortion for WCDMA handset applications," *IEEE J. Solid-State Circuit*, vol. 41, no. 5, pp. 1210–1221, May 2006.
[4] A. Ahmed, M. O. Abdalla, E. S. Mengistu, and G. Kompa, "Power amplifier modeling using memory polynomial with non-uniform delay taps," in *Proc. IEEE 34th European Microwave Conf. Proc.*, Amsterdam, The Netherlands, Oct. 2004, pp. 1457–1460.
[5] D. H. Kwon, H. Li, and Y. Chiu, "Adaptive digital techniques for efficiency and linearity enhancement of CMOS RF power amplifiers," *IEEE VLSI-DAT*, Apr. 2008, to be published.
[6] H. Besbes, T. Le-Ngoc, and H. Lin, "A fast adaptive polynomial predistorter for power amplifiers," in *Proc. IEEE Global Telecomm. Conf.*, Jul. 2001, vol. 1, pp. 659–663.
[7] Y. Nagata, "Linear amplification technique for digital mobile communication," in *Proc. IEEE Veh. Technol. Conf.*, San Francisco, CA, May 1989, pp. 159–164.
[8] J. K. Cavers, "Amplifier linearization using a digital predistorter with fast adaptation and low memory requirements," *IEEE Trans. Veh. Technol.*, vol. 39, no. 4, pp. 374–382, Nov. 1990.
[9] K. J. Muhonen, M. Kavehrad, and R. Krishnamoorthy, "Look-up table technique for adaptive digital predistortion: A development and comparison," *IEEE Trans. Veh. Technol.*, vol. 49, no. 9, pp. 1995–2002, Sep. 2000.
[10] Z. Rafik and B. Ridha, "A neural network pre-distorter for the compensation of HPA nonlinearity: Application to satellite communications," in *Proc. IEEE CCNC*, Jan. 2007, pp. 465–469.
[11] H. Durney and J. Sala, "CDF estimation for predistortion of non-linear high power amplifiers," in *IEEE Int. Conf. Acoust., Speech, Signal Process.*, May 2002, vol. 3, pp. 2545–2548.
[12] D. Huang, X. Huang, and H. Leung, "Nonlinear compensation of high power amplifier distortion for communication using a histogram-based method," *IEEE Tran. Signal Process.*, vol. 54, no. 11, pp. 4343–4351, Nov. 2006.
[13] K. C. Lee and P. Gardner, "Comparison of different adaptation algorithms for adaptive digital predistortion based on EDGE standard," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2001, vol. 2, pp. 1353–1356.
[14] K. Wesolowski *et al.*, "Efficient algorithm for adjustment of adaptive predistorter in OFDM transmitter," in *Proc. IEEE Veh. Technol. Conf.*, Sep. 2000, vol. 5, pp. 24–28.
[15] Intersil Inc., ILS5239 datasheet, Jul. 2002.
[16] Texas Instruments Inc., GC5322 datasheet, Mar. 2008.
[17] PMC-Sierra Inc., PM7820 product brief, 2006.
[18] Optichron, Inc., OP4400 product brief, Sep. 2007.
[19] P. Jardin and G. Baudoin, "Filter lookup table method for power amplifier linearization," *IEEE Trans. Veh. Technol.*, vol. 56, no. 3, pp. 1076–1087, May 2007.
[20] H. H. Chen, C. H. Lin, P. C. Huang, and J. T. Chen, "Joint polynomial and look-up table predistortion power amplifier linearization," *IEEE Trans. Circuits and Systems II*, vol. 53, no. 8, pp. 612–616, Aug. 2006.
[21] W. G. Jeon, K. H. Chang, and Y. S. Cho, "An adaptive data predistorter for compensation of nonlinear distortion in OFDM system," *IEEE Trans. Commun.*, vol. 45, no. 10, pp. 1167–1171, Oct. 1997.
[22] M. Jin, S. Kim, D. Ahn, D.-G. Oh, and J. M. Kim, "A fast LUT predistorter for power amplifier in OFDM systems," in *IEEE PIMRC*, Sep. 2003, vol. 2, pp. 1894–1897.
[23] K. Wesolowski and J. Pochmara, "Efficient algorithm for adjustment of adaptive predistroter in OFDM transmitter," in *Proc. IEEE VTC*, Sep. 2000, vol. 5, pp. 24–28.
[24] N. Naskas and Y. Papananos, "Non-iterative adaptive baseband predistorter for PA linearisation," *IEE Proc.-Microw. Antennas Propag.*, vol. 152, no. 2, pp. 103–110, April 2005.
[25] Wright and W. Durtler, "Experimental performance of an adaptive digital linearized power amplifier," *IEEE Trans. Veh. Technol.*, vol. 41, no. 4, pp. 395–400, Nov. 1992.
[26] D. Kim and S. Lee, "Analysis and design of an adaptive polynomial predistorter with the loop delay estimator," *Microw. Opt. Technol. Lett.*, vol. 34, no. 2, pp. 117–121, Jul. 2002.
[27] S. Tang, K. Gong, J. Wang, K. Peng, C. Pan, and Z. Yang, "Loop delay correction for adaptive digital linearization of power amplifiers," in *IEEE WCNC*, Mar. 2007, pp. 1987–1990.
[28] J. K. Cavers, "Optimum table spacing in predistorting amplifier linearizers," *IEEE Trans. Veh. Technol.*, vol. 48, no. 5, pp. 1699–1705, Sep. 1999.
[29] S. Haykin, *Adaptive Filter Theory*, 4th ed. Upper Saddle River, NJ: Prentice-Hall, 2002.
[30] L. Erup, F. M. Gardner, and R. A. Harris, "Interpolation in digital modems—Part II: Implementation and performance," *IEEE Trans. Commun.*, vol. 41, no. 6, pp. 998–1008, Jun. 1992.
[31] M. White, I. Mack, G. Borsuk, D. Lampe, and E. Kub, "Charge-coupled device(CCD) adaptive discrete analog signal processing," *IEEE Trans. Commun.*, vol. 27, no. 2, pp. 390–405, 1979.
[32] L. Deivasigamani, "A fast clipped-data LMS algorithm," *IEEE Trans. Acoust., Speech and Signal Process.*, vol. 30, pp. 648–649, 1982.

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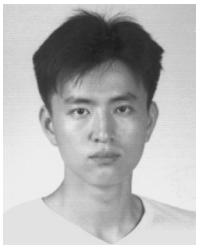

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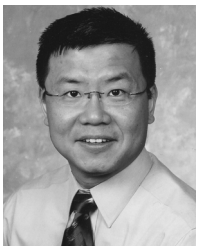

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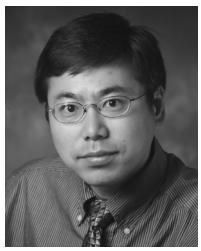

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