What Everyone Needs to Know about Carbon-Based Nanocircuits

Deming Chen, Scott Chilstedt, Chen Dong, and Eric Pop

Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign, IL, USA

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Department of Electrical and Computer Engineering
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Abstract— Sustained exponential growth of complex electronic systems will require new breakthroughs in fabrication and assembly with controlled engineering of nanoscale components. In this article, we describe an emerging class of transistors whose channels are made from semiconducting carbon nanomaterials. These nanomaterials come in two forms: carbon nanotubes (CNTs), and graphene nanoribbons (GNRs). The research community has given specific attention to these two carbon allotropes because of their outstanding electrical properties, including high mobilities at room temperature, high current densities, and micron-scale mean free paths. There are many possible transistor designs involving CNTs and GNRs, and each offers a unique set of benefits. They also face a number of challenges. This article covers the evolution of these designs, and highlights the works that have driven their development. It then introduces logic gates and small scale circuit structures that use these nanomaterial transistors. State of the art carbon nanomaterial modeling techniques and their application towards nanoscale VLSI circuit evaluation is discussed as well. At the end, we try to identify the opportunities and challenges involved in the adoption of carbon nanomaterials for building future electronics.

Index Terms— Nanotechnology, carbon nanotubes, graphene nanoribbons, nanomaterial transistors, nanoscale logic, nanocircuits design.

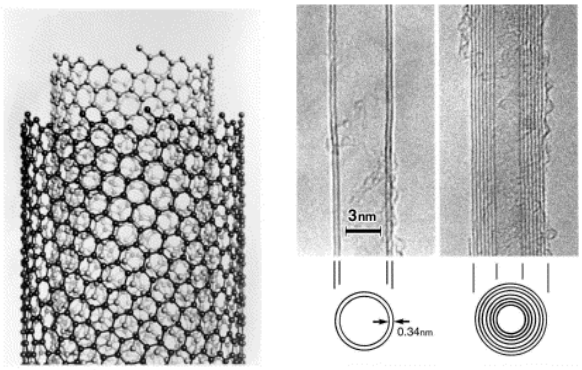
[1] The first three authors of this article have also written a book chapter, “Carbon Nanomaterial Transistors and Circuits”, to be published by Nova Science Publishers. Several sections of this article are based on content from that book chapter.

I. INTRODUCTION

Carbon is a group 14 element that resides above silicon in the periodic table. Like silicon and germanium, carbon has four electrons in its valence shell. In its most common state, it is an amorphous non-metal like coal or soot. In a crystalline, tetrahedrally bonded state, carbon becomes diamond, an insulator with relatively large band gap. However, when carbon atoms are arranged in crystalline structures composed of hexagonal benzene-like rings, they form a number of allotropes that offer exceptional electrical properties. For the replacement of silicon in future transistor channels, the two most promising of these allotropes are carbon nanotubes and graphene. In their semiconducting forms, these carbon nanomaterials exhibit room temperature mobilities over ten times greater than silicon. This translates to devices with significant improvements in performance and power savings, allowing higher integration at the same power density. In addition, they can be scaled to smaller feature sizes than silicon while maintaining their electrical properties. It is for these reasons that the Emerging Research Devices and Emerging Research Materials working groups of the ITRS (International Technology Roadmap for Semiconductors) have selected carbon-based nanoelectronics as their recommended “Beyond CMOS” technology [1].

A. Fundamentals of Carbon Nanomaterials

Carbon nanotubes can be categorized into two groups: single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs) (Figure 1). A SWCNT is a hollow cylinder with a diameter of roughly 1-4nm, and can be thought of as a rolled up sheet of monolayer graphene. A MWCNT is composed of a number of SWCNTs nested inside one another in order of diameter, and can be thought of as a rolled up sheet of multi-layer graphene. MWCNTs have dimensions greater than SWCNTs and are typically from four to several tens of nanometers in diameter. Carbon nanotubes vary in length and have been produced in lengths of up to 1 mm. With diameters of less than 10nm, this allows for exceptionally high aspect ratios, making nanotubes an essentially one-dimensional material.



(a) (b)

Figure 1. Multi-wall carbon nanotubes discovered in 1991: (a) schematic; (b) TEM image [4].

Due to their cylindrical symmetry, there is a discrete set of directions in which a graphene sheet can be rolled to form a SWCNT. To characterize each direction, two atoms in the graphene sheet are chosen, one of which serves the role of the origin. The sheet is rolled until the two atoms coincide. The vector pointing from the first atom to the second is called the chiral vector, and its length is equal to the circumference of the nanotube (Figure 2). The direction of the nanotube axis is perpendicular to the chiral vector.

The properties of a given SWCNT can be determined by its chiral vector (*n*, *m*). Depending on the rolling method, three different types of SWCNT can be synthesized: the *zigzag* nanotube with $m = 0$, the *armchair* nanotube with $m = n$, and *chiral* nanotubes with $n \neq m \neq 0$ (Figure 2(b)). MWCNTs are not characterized in this way because they are composed of nanotubes with varying chirality. Nanotubes can be either metallic or semiconducting depending on their chiral vector. If a CNT has a chiral vector where $m - n \neq 3x$ (x is an integer), it behaves as a semiconductor. The band gap varies inversely with single-wall carbon nanotube diameter, approximately as $E_G \approx 0.84/d$ eV, where d is given in nm.

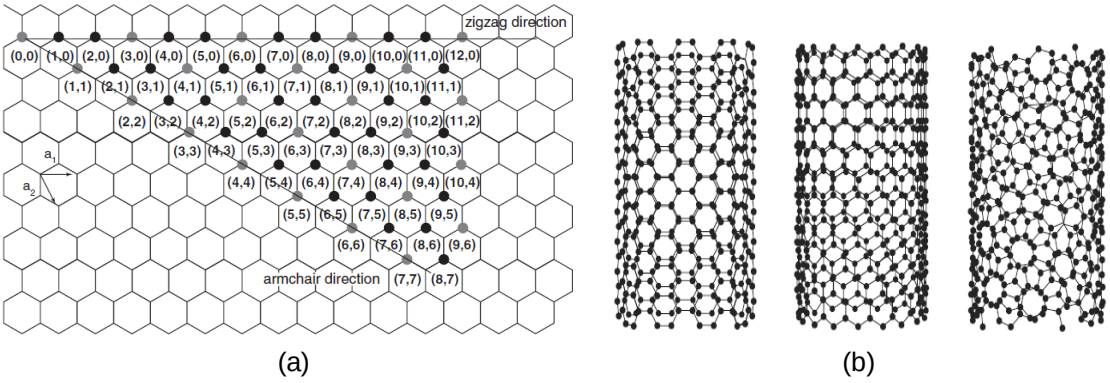


Figure 2. (a) Chiral vectors of SWCNTs. (b) SWCNT types: armchair, zigzag, chiral [5]

Like carbon nanotubes, graphene can exist in a number of forms. Monolayer graphene is made from a sheet of carbon exactly one atom thick, making it a pure two-dimensional material. Before graphene was first isolated in 2004, two-dimensional crystals were assumed to be too unstable to exist at room temperatures [3]. Since graphene does not wrap around and connect back to itself like a carbon nanotube, its edges are free to bond with other atoms. Because unbonded edges are unstable, the edges are usually found to be passivated by absorbents such as hydrogen. Other edge passivations include oxygen, hydroxyl groups, carboxyl groups, and ammonia [6].

Bulk planar graphene can be patterned by lithography to create narrow strips called graphene nanoribbons (GNRs). Such ribbons can also be created through techniques such as chemical synthesis [7] and the 'unzipping' of carbon nanotubes [8]. The smaller the width of the nanoribbon, the more impact the edge structure plays on its properties. The crystallographic orientation of the edges is especially important. Figure 3 demonstrates two possible edge state orientations, known as armchair and zigzag, and common width designations for each. In Figure 3(a), an armchair-GNR is shown with a size of $N = 10$, where N is the number of carbon atoms in width. In (b), a zigzag GNR is shown with a size of $N = 5$, where N is the number of zigzag chains in width.

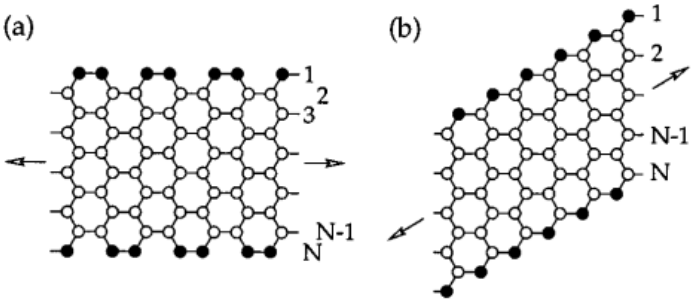


Figure 3. Graphene nanoribbon classification: (a) armchair, (b) zigzag [9].

B. Physical Properties

The regular crystalline structure of both graphene and carbon nanotubes gives them robust physical properties. For instance, the breaking strength of graphene has been measured as over 200 times greater than steel, making it the strongest material ever tested [10]. Due to the strength of the bonds in the graphitic lattice, carbon nanomaterials are stable at room temperature, and remain so even when scaled to atomic dimensions.

The strength and stability of carbon nanomaterials make them attractive for use in nanoelectronic devices that require stiffness, lightness, and robustness, such as NEMS (nano-electrical mechanical systems). They have also opened new opportunities in flexible electronics, since carbon-based devices can be flexed further without breaking than relatively rigid silicon devices. Even traditional electronics could see a benefit in the form of increased reliability in the face of environmental stresses such as mechanical shock.

Graphene and carbon nanotubes exhibit unusually high thermal conductivity [37][38], ~ 3000 $Wm^{-1}K^{-1}$, comparable to that of pure diamond and nearly an order of magnitude higher than copper. This allows them to dissipate the heat generated by electrical switching and device leakage more effectively, making them useful as thermal conduction paths in high density circuits. To this end, research is being done to investigate the viability of incorporating carbon-based thermal vias and channels for thermal management in present-day designs [39]. This application is especially important given the anticipated shift to thermally limited three-dimensional integrated circuits.

C. Low-Field Electrical Properties

The physical properties of carbon nanomaterials are obviously desirable, but the real opportunity lies in their electrical properties. While advances in silicon technology will certainly continue for the foreseeable future, a highly scaled silicon MOSFET will face formidable problems in terms of reduced drive current and increased short-channel effects such as drain-induced barrier lowering (DIBL). Carbon nanomaterials, on the other hand, have unique electrical properties that allow them to overcome these challenges and achieve strong performance at sub-10nm dimensions.

The high quality of the crystal lattice in carbon nanomaterials gives them a record-breaking mean free path, on the order of microns, which results in near-ballistic transport of charge carriers at low field in sub-micron devices. More importantly, this mean free path is achieved at room temperature, allowing for very high mobilities under practical operating conditions. In addition, owing to symmetric energy bands, the electron and hole mobilities are equal in both carbon nanotubes and graphene, unlike in other traditional semiconductors. Measured values of the mobility in nanotubes have recently been summarized in [40]. Studies have reported room temperature mobility up to 80,000 $cm^2/V{\cdot}s$ in pristine ultra-long carbon nanotubes [41]. However, it is important to point out that nanotube mobility scales not only with temperature ($\sim 1/T$), but also with nanotube diameter ($\sim D^2$) and with charge density. The roles of the latter two parameters have only been recently quantified through careful studies by [42][43], as summarized in Figure 4. In particular, the nanotube mobility at high charge density ($n > 0.5$ nm^{-1}) generally decreases as charge carriers begin to scatter within the second sub-band. Thus, under most practical operating conditions, the mobility in carbon nanotubes is expected to reach approximately ~10,000 $cm^2/V{\cdot}s$, still remaining an order of magnitude higher than in silicon.

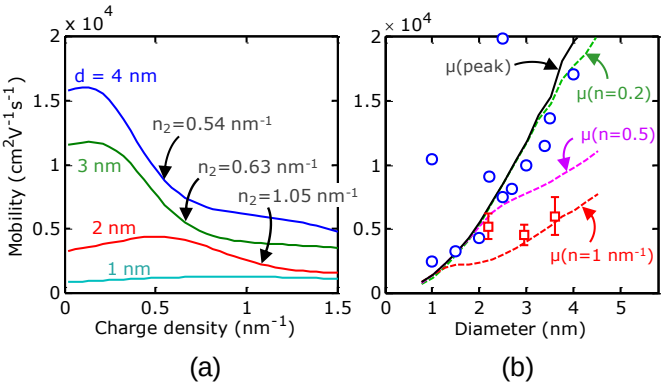


Figure 4. (a) Computed nanotube mobility vs. charge density for various diameters, at room temperature. The arrows indicate the charge densities where scattering with the second sub-band begins to dominate. (b) Computed mobility (lines) and experimental data (symbols) vs. nanotube diameter at various charge densities, and room temperature [43].

The mobility in most graphene samples on SiO_2 has been similarly measured at approximately 5,000-20,000 $cm^2/V{\cdot}s$ at room temperature [44], although values up to 120,000 $cm^2/V{\cdot}s$ have been recorded in *suspended* samples near room temperature (240 K) and low charge density ($2{\times}10^{11}$ cm^{-2}) [45]. Importantly, as the carrier density increases, mobility decreases in monolayer graphene, while it increases in bilayer and trilayer graphene [46]. In addition, when graphene is placed on a substrate, the vibrations of the dielectric (e.g., SiO_2) are transferred to the carbon lattice, causing remote interfacial phonon scattering [11], and decreasing the mobility. Nevertheless, even with such effects, room temperature mobilities over ten times greater than silicon have been routinely achieved, while experiments on suspended samples hint at the upper limits that may be physically possible. Such mobility results in high carrier velocities, low conductance, and the possibility of terahertz-speed devices.

D. High-Field Electrical Properties

Conventional semiconductors display velocity saturation effects at high electric fields, from strong scattering with lattice vibrations. For instance, in silicon the average carrier velocity at fields >1 V/μm saturates at approximately $v_{sat} \approx 10^7$ cm/s, and is independent of temperature and carrier density [47]. Unlike silicon, the velocity saturation in carbon nanotubes and graphene is higher, yet dependent on carrier density, scaling inversely with it due to the particular band structure. For instance, in carbon nanotubes $v_{sat} \approx 4{\times}10^7$ cm/s at low carrier density (~0.1 nm^{-1}), and decreases in half to ~$2{\times}10^7$ cm/s at high carrier density (~1 nm^{-1}) [48]. In graphene, the velocity saturation also scales inversely with charge density. Values between $5.5{\times}10^7$ cm/s (at ~$5{\times}10^{11}$ cm^{-2} carrier density) and $6.3{\times}10^6$ cm/s (at ~10^{13} cm^{-2} carrier density) have been estimated from high-field experiments [49].

Another important high-field characteristic of such devices is the effect of Joule heating, which cannot be ignored particularly for carbon devices placed on a good thermal insulator such as SiO_2. Temperature rise of >100 ^oC is easily reached in metallic carbon nanotubes on SiO_2 at just ~0.1 mW power input (e.g., 20 μA at 5 V), and if the voltage is further increased the nanotubes typically break by oxidation, as shown in Figure 5(a) [50]. In this case, the poor thermal conductance of the SiO_2 insulator and of the nanotube-SiO_2 interface will dominate heat sinking, despite the good thermal conductivity of the nanotube itself. Unlike in metallic nanotubes, semiconducting nanotubes display an additional phenomenon at high fields. Due to the presence of a band gap, electron-hole pair creation can be favored over phonon scattering (and heat dissipation), leading to a remarkable current increase at high voltages, as shown in Figure 5(b) and (c). The latter was a phenomenon recently

reported [51], and could be used as a highly non-linear transistor switching mechanism in and of itself, as has been previously done with avalanche-based silicon transistors [52]. However, the avalanche fields in carbon nanotubes have been estimated as smaller by an order of magnitude than those in silicon, leading to additional advantages in terms of lower voltage operation.

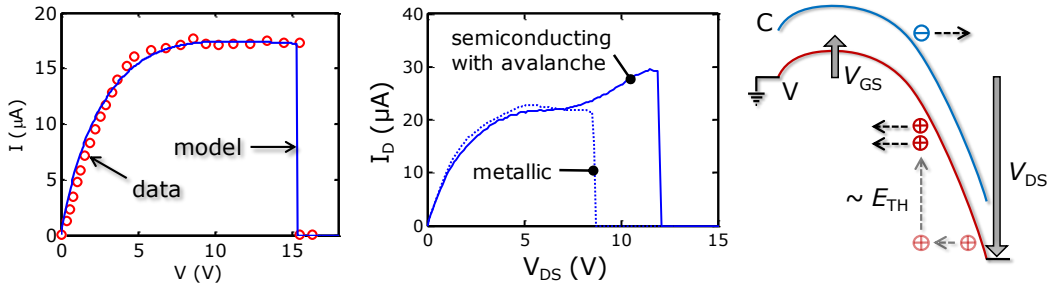


Figure 5. High-field effects in carbon nanotubes. (a) Current saturation due to Joule heating in long metallic nanotubes [50]. The nanotube reaches ~900 ºC when breakdown by oxidation occurs. (b) Current increase in semiconducting nanotubes at high fields (>2 V/μm), due to avalanche impact ionization [51]. (c) Schematic band diagram of the avalanche process.

II. CARBON NANOTUBE FETS (CNFETS)

The first reports of operational room-temperature CNFETs came in 1998 from groups at IBM [12] and Delft University of Technology (TUDelft) [13]. The structures of the two CNFET devices are shown in Figure 6. These designs have similar architectures: a single nanotube (either single-walled or multi-walled) behaves as the channel region and rests on metal source/drain electrodes. The design from [12] has a 140nm thick SiO_2 dielectric on top of a silicon back gate and 30nm thick Au electrodes defined by e-beam lithography; whereas the design from [13] uses Pt electrodes with a 300nm thick SiO_2 insulator. Au and Pt contacts are selected because their work functions are close to the carbon nanotube work function of 4.5eV.

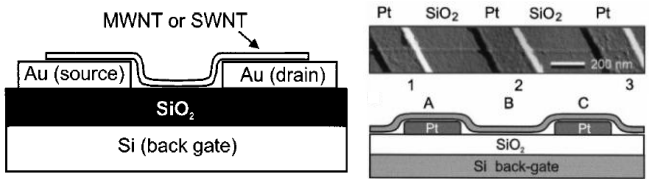
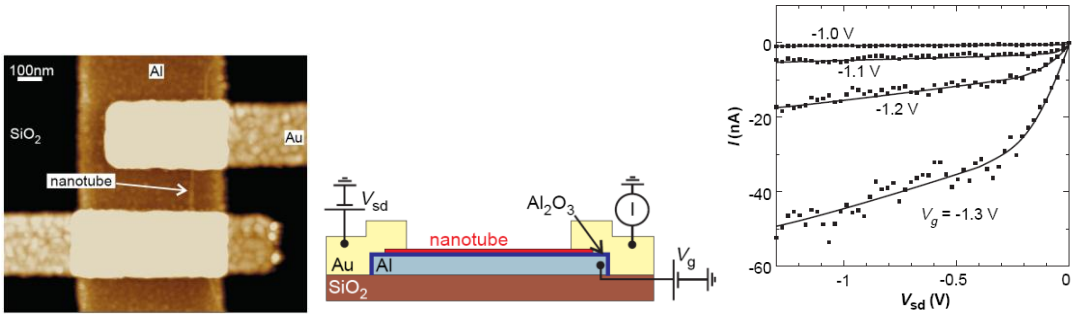


Figure 6. Schematic cross section of Si back gated CNFET (a) with Au S/D contacts [12], (b) with Pt S/D contacts [13].

These pioneering works successfully demonstrated the CNFET as a promising switch for future integrated circuit design. However, it is difficult to integrate multiple-device circuits based on the layouts in Figure 6, because the silicon substrate is used as a back gate. This means that the same gate voltage is applied to all of the devices on that substrate, requiring the use of a substrate isolation technique such as shallow trench isolation (STI).

In 2001, the group from TUDelft enhanced their previous CNFET design by using aluminum local gates to control individual transistors, as shown in Figure 7(a)-(b) [14]. This design uses a narrow Al gate and is insulated by thin native Al_2O_3. The Al gate is defined by e-beam lithography on silicon oxide, and the gate insulator is grown by exposing the Al gate to air. Single-wall nanotubes are

then deposited onto the wafer on top of the predefined gates. Finally, Au source and drain contacts are created by e-beam lithography. The device I-V_{SD} characteristic is plotted in Figure 7(c), and shows that this new CNFET works as an enhancement-mode p-type device.

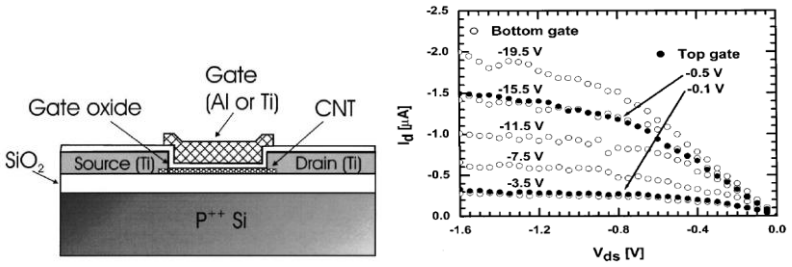


(a) (b) (c)

Figure 7. (a) AFM image of a single-nanotube transistor. (b) CNFET with individual Al back gate. (c) I-V_{SD} characteristic [14].

In order to build logic functions, it is necessary to have both n-type and p-type transistors available. However, all of the aforementioned CNFETs are p-type. Results in [15] demonstrate that n-type CNFETs can be obtained by annealing of a p-type device or through doping.

A major improvement of carbon nanotube devices was made in 2002 through the creation of an MOS structure with a gate electrode on top of the nanotube channel and separated by a thin layer of SiO_2 dielectric. The structure of this top gate design resembles common silicon MOSFET designs and is shown in Figure 8. Top-gated designs offer several important improvements over back-gated devices. First, back-gated devices use a relative thick ~100nm oxidation layer which requires a high gate voltage to switch the device on. On the other hand, top-gated CNFETs can have a thin gate dielectric of 15~20nm, allowing for operation at lower voltage. Second, top gating dramatically reduces the gate source/drain overlap capacitance which is critical to high-frequency operation. In addition, with back-gated devices, the carbon nanotubes are exposed to air. Such exposure can cause the n-type devices obtained from previously mentioned techniques to revert back to p-type. In top-gated devices, the carbon nanotubes are encapsulated in gate oxide, avoiding this electrostatic instability problem and helping to improve reliability.



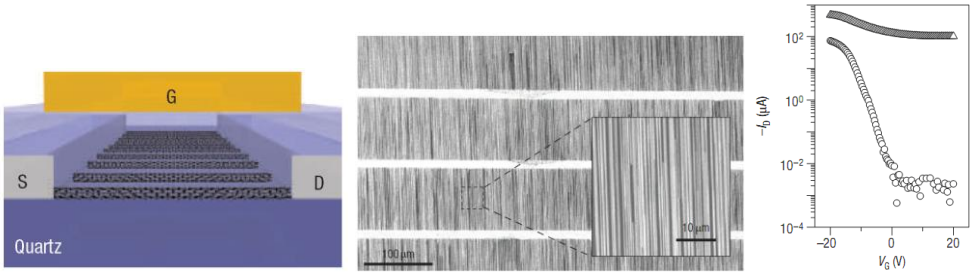
(a) (b)

Figure 8. Top-gated CNFET (a) device structure; (b) IV comparison to back-gated device [16].

Another top-gated CNFET design was presented in [16]. In this design, the CNT is fabricated on top of a heavily doped single-crystal silicon wafer coated with 120nm of thermal SiO_2. The operating voltages of the top-gated device are much lower (-0.1V ~ -0.5V over threshold) than for bottom-gated counterparts (-3.5V ~ -15.5V over threshold). Meanwhile, integration of thin films of ZrO_2 high-k dielectrics into CNFETs has been demonstrated in [17]. Using a high-k gate insulator, normalized

CNFET transconductance and carrier mobility of 3,000 Sm^{-1} and 3,000 $cm^2V^{-1}s^{-1}$, respectively, was achieved. Compared to a 60nm Intel MOSFET with transconductance 800 Sm^{-1}, a high-k CNFET offers over a threefold improvement. High-k CNFET devices have been reported to have excellent subthreshold swing as well.

Single nanotube devices reveal great performance improvements over existing solutions. However, the integration of a single tube into existing integrated circuits is still a great challenge. Due to limited fabrication control of nanotube properties, a single CNT device is susceptible to large performance fluctuations. One feasible solution is to use densely packed, horizontal arrays of non-overlapping SWCNTs in the channel, as shown in Figure 9(a) [19]. This creates parallel conducting paths that can provide larger current than a lone CNT. Having multiple carbon nanotubes in the channel also statistically averages the device-to-device variation and offers increased reliability against a single tube failure.



(a) (b) (c)

Figure 9. (a) Cross section of a CNFET with a channel of multiple parallel nanotubes. (b) Dense arrays of SWCNTs. (c) Transistor IV curve before and after metallic CNT removal [19].

There are two major challenges in fabricating a multiple carbon nanotube device, both of which have been addressed in [19]. The first challenge is the creation of large-scale, high-density, perfectly aligned nanotube arrays. These can be achieved by using photolithography-defined parallel patterns on a quartz surface and growing carbon nanotubes with CVD along these predefined patterns. Using this technique, nanotube arrays can be successfully fabricated with average diameters of ~1nm and lengths over 300um, with 99.9% alignment (Figure 9(b)). The nanotubes can then be transferred to the desired substrate, such as silicon or even a flexible plastic.

The second challenge is that intrinsically, one third of the fabricated carbon nanotubes are metallic. The metallic carbon nanotubes cannot be controlled by gate voltage and are always conducting, which deteriorates the transistor on/off ratio. Metallic nanotubes can be removed by techniques such as electrical breakdown [20]. Figure 9(c) demonstrates that after the electrical breakdown process, Ion/Ioff ratios can be improved by four orders of magnitude. Recently, a new technique, VLSI-compatible Metallic-CNT Removal (VMR), combines layout design with CNFET processing and is able to efficiently remove metallic-CNTs in the circuit at the chip scale. As a result, VMR enables the first experimental demonstration of complex cascaded CNFET logic circuits and represents a promising fabrication technique for large-scale CNT-based circuits [21].

III. GRAPHENE NANORIBBON FETS (GNRFETS)

The intrinsic physical and electrical properties of graphene make it desirable for a large number of potential applications ranging from biosensors to flexible electronics to solar cell electrodes. One of the most exciting applications is the use of graphene channels in future high-performance transistors. To that end, physicists and materials scientists have been characterizing and experimenting with graphene to understand how it could be used to make such devices a reality.

Few-layer graphene was initially discovered at the University of Manchester in 2004 (Figure 10(a)-(c)) [22]. The first graphene transistor-like device was created shortly thereafter, a simple test structure constructed to measure graphene's field effect behavior (Figure 10(d)-(e)).

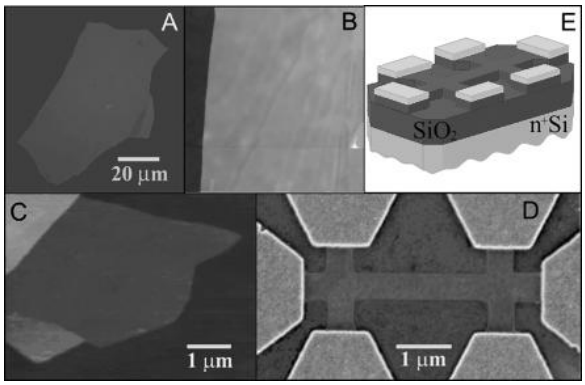


Figure 10. (a)-(c) First images of few-layer graphene. (d)-(e) Test structure [22].

The major challenge with graphene is that in its native state as a large sheet, it behaves like a zero-band gap semiconductor, or semi-metal, meaning that it conducts electrons freely. This is desirable if graphene is to be used for interconnect, and of course many researchers are exploring this possibility. However, in order to be effective for use in transistors, graphene needs to be made semiconducting and demonstrate a high on/off ratio. To obtain the necessary off state, a band gap must be introduced.

One way to open a band gap is to pattern graphene into a narrow ribbon to laterally confine the charge carriers in a quasi-one-dimensional system somewhat analogous to a CNT. This idea was experimentally demonstrated in [23], where researchers at Columbia University used e-beam lithography to define two dozen graphene nanoribbons with widths ranging from 10-100nm and varying crystallographic orientations. Conductance of these GNRs was measured at both 300 K and 1.6 K. The measurements show that for a given crystallographic direction, the energy gap depends strongly on the width of the GNR. As the ribbons are made smaller, less conductance is observed, which indicates a stronger semiconducting behavior. A similar experiment in [24] comes to a similar conclusion. In both cases, researchers also note an apparent dependence of the electrical behavior on the edge states of the nanoribbons.

One of the first works to demonstrate sub-10nm width GNRFETs was [29]. The authors were able to achieve such dimensions because instead of patterning GNRs from a planar sheet with e-beam lithography, they started with GNRs that had been chemically derived at smaller dimensions using the process described in [7]. In this process, exfoliated graphene is dispersed into a chemical solution by sonification, creating very small fragments. The solution is then applied to a substrate and dried, and GNRs are identified with atomic force microscopy. These GNRs ranged from monolayer to trilayer, and were deposited on a SiO_2 dielectric over a highly doped silicon back gate, and contacted with Pd source/drain electrodes. A schematic of this design is shown in Figure 11(a). A number of devices were created using the bilayer GNRs, including both wide (10-60nm) and small (< 10nm) GNRFETs. When tested, all of the large GNRs demonstrated metallic behavior due to vanishingly small band gaps, while all of the sub-10nm GNRFETs were found to be semiconducting. Atomic force microscopy (AFM) images of two example devices are shown in Figure 11(b-c). Compared to the earlier works on GNR with 20nm width [18], the semiconducting GNRFETs show 10^5 higher I_{on}/I_{off} ratio at room temperature, ~20 times higher current density (at V_{ds} = 1V), and ~100 times higher transconductance per μm. This is due to larger band gaps, higher GNR quality, thinner gate oxide, and shorter GNR channel [29].

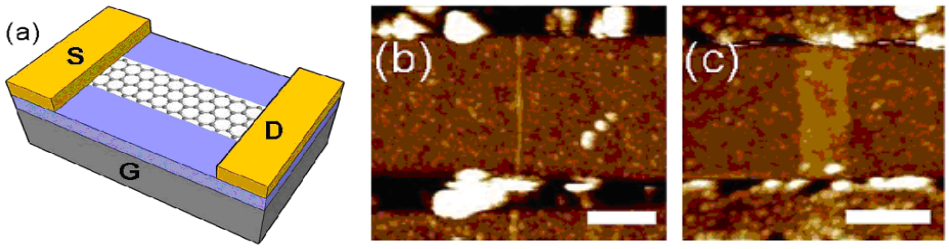


Figure 11. Back gated GNRFET: (a) schematic; (b) AFM image with w ~ 2 ± 0.5nm; (c) AFM image of GNR with w ~ 60 ± 5nm [29].

The importance of GNR edge states was predicted by first-principles physics calculations [9][25]. A recent experimental work used scanning tunneling microscopy to verify this prediction, confirming that the crystallographic orientation of the edges significantly influences the electronic properties of nanometer-sized graphene [26]. By measuring the band gap of graphene samples and noting their predominant edge chirality, they observed that nanoribbons with predominantly-zigzag edges are metallic, while predominantly-armchair edges are semiconducting [26]. For GNR transistors, all-semiconducting armchair edges are the most desirable. However, in the ribbons produced so far, the edges are not always atomically smooth and often contain a mixture of segment types, as seen in Figure 12. In these cases, the semiconducting properties weaken, and the band gap becomes dependent on the ratio of armchair segments to zigzag segments [26].

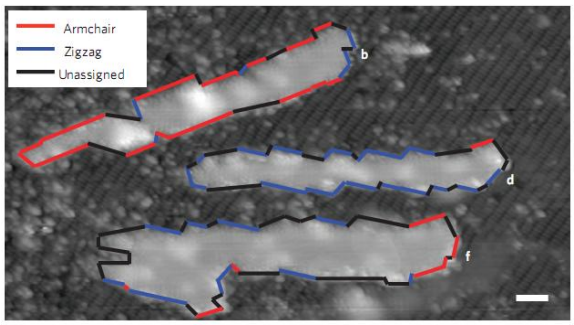


Figure 12. GNR with different dominant edge chiralities. Top: Armchair GNR with 0.38eV band gap. Middle: Zigzag GNR with 0.14eV band gap. Bottom: Zigzag GNR with 0.12eV band gap) [26].

In addition to logic applications, GNRFETs are well suited for individual ultrahigh-frequency analog transistors [27]. Top-gated graphene transistors of various gate lengths have been fabricated with peak cutoff frequencies up to 26 GHz for a 150nm gate [28]. Results also indicate that if the high mobility of graphene can be preserved during the device fabrication process, a cutoff frequency approaching terahertz may be achieved for graphene FETs with a gate length of just 50nm and carrier mobility of 2000 $cm^2/(V \cdot s)$ [27][28].

IV. LOGIC GATES AND CIRCUIT STRUCTURES

In order to be useful to the semiconductor industry, transistors must be connected together to form higher-order circuits. Because carbon nanomaterials exhibit different characteristics, alternate logic families to static CMOS can be considered.

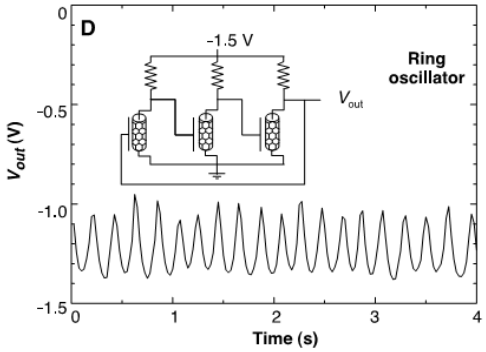


Figure 13. CNFET ring oscillator implemented in resistor-transistor logic [14].

A. CNFET Logic Structures

The first CNFET logic gates were demonstrated in [14]. A range of digital logic operations and building blocks were demonstrated, including an inverter, a NOR gate, an SRAM cell, and an AC ring oscillator consisting of one, two, and three-transistor circuits. These gates were implemented using resistor-transistor logic, in which the p-type CNFETs were connected to large off-chip resistors. The ring oscillator was implemented by connecting three inverters in series, as shown in Figure 13, and achieved an operating frequency of 5Hz. This low frequency was due to the gigaohm resistance and 100pF parasitic capacitance of the wires connecting to the off-chip bias resistors.

The performance of CNFET ring oscillators was enhanced in a following work by [30]. In this work, SWCNT arrays were synthesized by chemical vapor deposition (CVD) on substrates pre-patterned with catalyst, and local gating was obtained by using tungsten metal back gates. More importantly, local doping was applied to convert p-type CNFETs into n-type, allowing complementary CNFET logic to be created for the first time. The resulting three-stage ring oscillator had a measured frequency of 220 Hz, much higher than previously achieved with resistor-transistor logic. This speed can be further optimized by reducing the resistance of electrode to carbon nanotube contacts and the parasitic capacitance of the interconnect.

Recently, a multi-stage top-gated complementary CNFET ring oscillator was built on a single 18-mm-long SWCNT [31]. This ring oscillator consists of 12 individual CNFETs: six p-type FETs with Pd metal gates and six n-type FETs with Al metal gates. Five inverter stages were used for oscillation and another inverter was used for reading the signal. A frequency response of 52 MHz was measured. This frequency was still limited by the parasitics rather than by the intrinsic nanotube speed.

Large-scale integration requires the creation of nanotubes at wafer scale, as well as precise directional control to allow parallel CNT arrays for high density logic. In [32], researchers from Stanford University presented techniques for addressing this challenge. First, they demonstrated wafer-scale growth of SWCNTs on a quartz substrate. Then, they detailed the wafer-scale transfer of the CNT arrays on to a silicon substrate using a process based on thermal release tape. Arrays of standalone logic gates are then fabricated through photolithography. Although the CNTs are aligned to the crystal orientation of the single-crystal quartz substrate on which they are grown, a very small fraction of CNTs may be misaligned during growth or become misaligned during the transfer process. This misalignment can cause shorts between transistor source and drain (Figure 14(a)), reducing the on/off ratio of the gate and possibly causing incorrect gate logic.

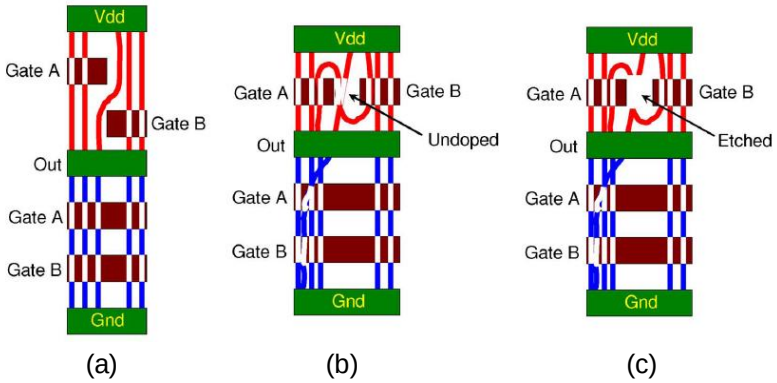


Figure 14. (a) Misaligned CNT. (b)-(c) Misalignment-immune techniques [33].

To address this problem, a misalignment-immune logic design strategy is presented in [32] and [33]. This technique allows CNT circuits to be created on imperfect CNT arrays. To illustrate this, three possible gate structures for a NAND gate are shown in Figure 14. Design (a) has the two pull-up gates at different horizontal levels to create a compact layout in the horizontal direction. Designs (b) and (c), on the other hand, have the two pull-up network gates at the same horizontal level, and separate them by either an undoped region (b) or an etched region (c). Ideally, all CNTs should be grown perfectly aligned and pass underneath the gates, however as shown in (a), misaligned CNTs can short source and drain, creating incorrect logic functions. Designs (b) and (c) are immune to this problem because the section of misaligned CNTs that do not pass through the gates is either undoped or etched away, which means it will not be conducting. This design technique reveals a possible new research direction for computer-aided design tools: CNFET circuit designs could be made misalignment immune by automatically inserting undoped/etching regions where misalignment defects could cause faults.

B. GNRFET Logic Structures

The first inverter based on integrating two graphene transistors of opposite types was presented in [34]. The two GNRFETs were produced on a single flake of monolayer graphene as shown in Figure 15(b). The left-hand transistor in Figure 15(a) was electrically annealed to obtain an n-type FET while the right-hand transistor contained a pristine p-type FET. The transistors were back-gated by a highly doped silicon substrate insulated with a layer of SiO_2.

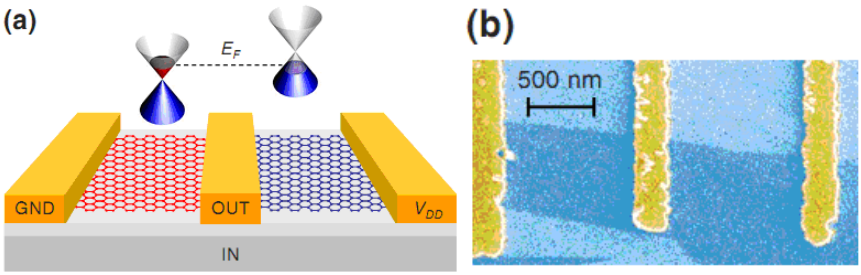


Figure 15. Complementary GNRFET inverter: (a) design; and (b) SEM image [34].

Another graphene logic family is presented in [35]. This design takes advantage of the observations that GNRFETs do not exhibit drain current saturation effects, and instead behave as simple voltage controlled resistors whose resistance depends only on the applied gate voltage. This means that small changes in the gate input voltage can be detected by measuring the resulting

source-drain resistance. By taking two input signals and using the average of them to drive the gate voltage, the state of the two input signals can be determined by the corresponding output resistance of the transistor. By using the small signal response of the drain voltage in response to the varying gate voltages, logical output signals were derived for XOR, NAND, OR, and NOT functions using a two terminal GNRFET. The main drawback of this design is that the gates would be very susceptible to noise and variations, as the logical values depend on fractional changes to the gate input voltage. Another problem is that the gate is always conducting, and hence constantly consuming static power. This power dissipation could be reduced by using a graphene transistor with a high resistance, but this would decrease the speed of the gate [35].

Recent developments in the use of growth on copper foils and films have produced promising results. In [2], a technique was demonstrated that produces 1cm single layer graphene (SLG) on copper films, and patterning GNRFETs on this layer (Figure 16). This allows direct fabrication of uniform transistor arrays using known thin film technology, without the need for delicate transfer processes. Furthermore, the devices demonstrated a low failure rate (<5%), and uniform electrical properties [2]. This development helps to realize the primary advantage of graphene over carbon nanotubes: the ability to be fabricated using planar processing techniques that can easily be streamlined and automated.

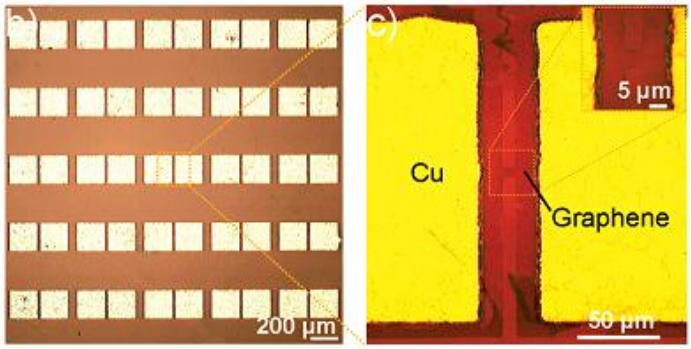


Figure 16. Array of field effect transistors fabricated on monolayer graphene.

V. LARGE-SCALE INTEGRATION

Despite the large number of nanomaterial-based devices that have been proposed, there are relatively few that have specifically focused on carbon-nanomaterial based architecture designs. In the work [36], a CNT-based FPGA architecture was proposed and evaluated using CNFET transistor models, SPICE simulations, and a CAD flow. This proposed architecture uses arrays of multiple-tube top-gated CNFETs to form the memory decoder in FPGA lookup tables, and uses metallic CNTs to build nanotube-based memories. To account for variations in nanoscale fabrication such as the number of CNTs in a FET channel, a variation-aware CAD flow was developed [36]. Figure 17 shows the concept of the design. It uses parallel ribbons of SWCNTs held in place by metal electrodes and crossed by metal gates. PMOS CNFET devices are formed at the crossing points of the CNT ribbons and the metal gates, creating a CNFET decoder. At points where the CNT ribbons pass over a trench in the substrate, NRAM memory devices are formed. This CNT memory is used to store the truth table of the so-called basic logic element's logic function. By applying K inputs to the decoder, a reading voltage will be sent to the corresponding memory bit whose output can then be read from the base electrode. One of the advantages of this LUT design is that it builds the decoding and memory on the same continuous CNT ribbons. This structure allows for high logic density and simplifies the manufacturing process.

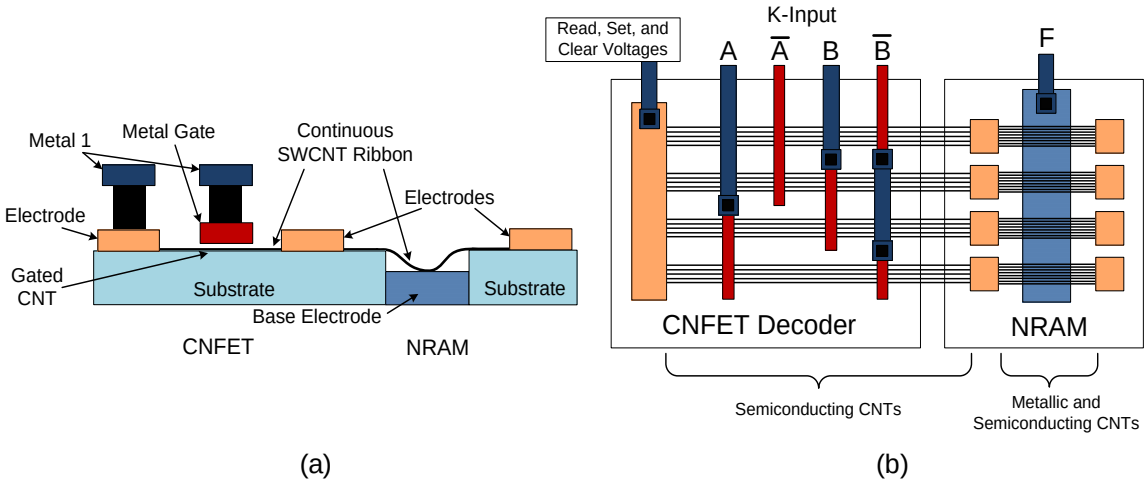


Figure 17. CNT-based LUT design. (a) Cross section of one nanotube ribbon. (b) Layout of a 2-input LUT design [36].

While works like this represent a good start, much more research is needed to determine the best circuit designs, architectures, and CAD techniques to fully exploit carbon nanomaterials in real applications and systems.

VI. CHALLENGES AND OPPORTUNITIES

Carbon nanomaterials offer many advantages for integrated electronics, but a number of hurdles must be overcome before CNFETs and GNRFETs can be used in large-scale integration. The first of such challenges is the construction of the nanomaterials themselves. The major issue in CNFET development is the lack of a controlled growth process to achieve prescribed chirality, conductivity, diameter, and number of walls. As a result metallic and semi-conducting nanotubes are mixed together after synthesis. Although post-processing techniques such as electrical breakdown can help, a fully controlled carbon nanotube synthesis recipe needs to be developed to create low-cost, high-quality semiconducting nanotubes with small process variation. Then, even if the type of CNT can be predetermined, techniques need to be developed to control the location and alignment of the CNTs on the target wafer.

The second challenge that has yet to be solved is the hybrid fabrication of carbon nanomaterials and CMOS components, and the interfacing of small nanomaterial transistors with larger devices. Similarly, the major issue in the development of graphene has been the lack of a reasonable process for growing graphene epitaxially on a suitable substrate. Most of the known large-scale fabrication techniques yield areas that contain a varying mix of monolayer, bilayer, trilayer, and many-layer graphene.

Even if controlled defect-free carbon nanomaterial synthesis can be achieved, further challenges must also be addressed. In order to obtain uniform performance among GNRFETs, advanced patterning techniques will be needed to define GNRs with known width, edge smoothness, and chirality. If atomically smooth edges are desired, sub-nanometer resolution patterning will be needed. This can be effective at minimizing variation, but will probably never remove it completely. In graphene, differences in edge doping, lattice defects, oxide thicknesses, and ripples in the graphene sheets will still contribute to device variation. Likewise, CNTs will have to worry about differences in alignment, tube chiral vectors, diameters, and doping. Therefore, variation-aware and fault-tolerant design techniques will need to be heavily employed.

A major opportunity lies in the development of advanced modeling techniques. With accurate CNFET and GNRFET models and fast simulators, high-level circuit and architecture design spaces could be more quickly explored. Such results could be used to determine the most promising directions for future development and help guide research on device fabrication.

There are serious attempts to commercialize nanomaterial-based electronic products. Examples include the effort carried out by the startup company Nantero [53] to build nanotube-based memory (NRAM) and by the new startup company NuPGA [54] that uses graphite in the vias as a fuse to build FPGAs. We expect that in six to eight years, carbon nanomaterial-based electronics will appear, one way or another, in the market; that is when silicon-based solutions reach scaling limits, and new materials and process technologies will be required to further the continuation of Moore's Law.

VII. CONCLUSIONS

The future of the IC industry is not as clear-cut today as it was a decade or two ago. As circuits move to smaller dimensions, the traditional silicon CMOS design is losing its appeal, and alternative materials are being considered. Carbon nanomaterials have been identified as potential candidates to replace silicon in high-speed, low-power device channels. The record-breaking electrical and physical properties of carbon nanotubes and graphene make them attractive for use in such applications, but the practicality of such devices is still unclear. In this article, we have reviewed the latest research on carbon nanotube FETs and graphene nanoribbon FETs. This provides an early look at the unique opportunities that these devices present, and helps to identify key problems and research directions that must be addressed before carbon nanomaterials can see widespread adoption.

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