Deming Chen

410 Coordinated Science Laboratory
1308 W. Main St.
University of Illinois, Urbana, Illinois 61801

Office: 217-244-3922
dchen@illinois.edu
http://dchen.ece.illinois.edu/

Education

B. S. Physical Chemistry	Amoy (Xiamen) University, Xiamen, China, 1990
B. S. Computer Science	University of Pittsburgh, Pittsburgh, 1995
M. S. Computer Science	University of California, Los Angeles, 2001
Ph. D. Computer Science	University of California, Los Angeles, 2005

Current and Previous Academic Positions

Aug. 2015 – present	Professor, Donald Biggar Willett Faculty Scholar
Aug. 2011 – 2015	Associate Professor
Aug. 2005 – 2011	Assistant Professor Department of Electrical and Computer Engineering University of Illinois, Urbana-Champaign
Aug. 2015 – present	Affiliate Professor (0%)
Aug. 2011 – 2015	Affiliate Associate Professor (0%)
Aug. 2008 – 2011	Affiliate Assistant Professor (0%) Computer Science Department & Coordinated Science Lab University of Illinois, Urbana-Champaign

Other Professional Experiences

Jun. 2016 – present	President and Co-founder, Inspirit IoT, Inc. Champaign, Illinois
Mar. 2001 – Jul. 2002	Software Engineer, Aplus Design Technologies, Inc. Los Angeles, California
Jul. 1995 – Sep. 1999	System Engineer, Applied Systems Associates, Inc. Murrysville, Pennsylvania
Sep. 1990 – Sep. 1991	Research Staff, Institute of Coal Chemistry Chinese Academy of Sciences, China

Visiting or Seconded Positions

Jul. 2012 – Sep. 2012	Visiting Associate Professor Center for Energy-Efficient Computing and Applications Peking University, China
Oct. 2012 – Dec. 2012	Visiting Associate Professor Department of Electrical Engineering Stanford University, USA

Mar. 2010 – Present	Seconded faculty appointment Advanced Digital Sciences Center (ADSC), Singapore

Short Summary

Deming Chen has published more than 180 refereed journal and conference papers, and book or book chapters in the areas of FPGA (synthesis, computing, architecture), EDA (system-level/high-level/logic synthesis), Machine Learning (acceleration, IoT system, algorithm), Heterogeneous Computing (hybrid systems of CPU/FPGA/GPU), and Nanotechnology (device modeling and nano-circuits). In recent years, he also actively pursued other research directions such as computational genomics and hardware security. His research has generated high impact. For example, he led a group of researchers and developed a new DNA error correction tool, called *BLESS*, which has been downloaded for almost 3000 times from ~60 countries since January 2014 when the corresponding paper was published in the journal *Bioinformatics*. He has also been leading the *FCUDA* project (the CUDA-to-FPGA compiler) since 2008. This package is open source now to benefit both the industrial and academic communities. He has served as PI/Co-PI on more than 30 research grants administered by US Federal agencies as well as industry. In addition, he has been a seconded faculty member for the Illinois ADSC center in Singapore since March 2010, supervising a research group there. He has received eight Best Paper Awards (ASPDAC'09, SASP'09, FCCM'11, SAAHPC'11, CODES+ISSS'13, ICCAD'15, SLIP'18, and ICCAD'18) and numerous other awards. He has served as an Associate Editor for several leading journals, and as General Chair, Program Chair, Track/Subcommittee Chair, or TPC member for many important conferences in his research areas. He has extensive industrial experience. In 2001, he joined Aplus Design Technologies and commercialized his published algorithm on CPLD technology mapping, and the software was exclusively licensed by Altera (now part of Intel) and distributed to many customers worldwide. He is one of the inventors of the xPilot High-level Synthesis package developed at UCLA, which was licensed to AutoESL Design Technologies, Inc. Currently, he is the President and Chairman of the Board for a new startup Inspirit IoT, Inc., headquartered in the Research Park at Champaign, IL. He also actively provides consulting services or short courses for leading semiconductor or FPGA computing companies. He is the Donald Biggar Willett Faculty Scholar of College of Engineering, an IEEE Fellow, an ACM Distinguished Speaker, and the Editor-in-Chief of ACM Transactions on Reconfigurable Technology and Systems (TRETS).

Awards and Honors

- Achievement Award for Excellent Teamwork, Aplus Design Technologies, Inc, 2001
- "Power Modeling and Characteristics of Field Programmable Gate Arrays" – one of the most-downloaded articles from IEEE Transactions on CAD, 2006
- Strathmore's Who's Who, 2007-2008
- Arnold O. Beckman Research Award, UIUC, 2007
- NSF Career Award, 2008
- Included in the List of Teachers Ranked as Excellent, Spring 2008
- Best Paper Award, IEEE/ACM Asia and South Pacific Design Automation Conference, 2009
- Best Paper Award, IEEE Symposium on Application Specific Processors, 2009
- ACM SIGDA Outstanding New Faculty Award, 2010
- Best Paper Award, IEEE International Symposium on Field-Programmable Custom Computing Machines, 2011
- Best Paper Award, Symposium on Application Accelerators in High Performance Computing, 2011
- Senior member of IEEE, 2011
- Best Paper Award Nomination, IEEE International Conference on Field-Programmable Technology, 2011

- Best Paper Award, IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2013
- 10-Year Retrospective Most Influential Paper Award Nomination, IEEE/ACM Asia and South Pacific Design Automation Conference, 2014
- IBM Faculty Award, 2014, 2015
- Keynote speech, IEEE International Conference on Anti-counterfeiting, Security, and Identification, 2014
- Distinguished Visiting Professor, 2015-2017, Fudan University, China
- Donald Biggar Willett Faculty Scholar, College of Engineering, University of Illinois, 2015
- Keynote speech, IEEE International Conference on ASIC, 2015
- Best Paper Award, IEEE/ACM International Conference on Computer-Aided Design, 2015
- Distinguished Service Award, ACM, 2016
- Keynote paper, *Integration, the VLSI Journal*, 2016
- NSF SBIR (Small Business Innovation Research) Award, with Inspirit IoT, Inc., 2017
- First Place Winner, International Hardware Design Contest on IoT, Design Automation Conference, 2017
- Invited Speaker, ICC Distinguished Lecture Series, Michigan Tech, 2017
- Invited Distinguished Speaker, Masters & Robots Conference, 2017
- Student Best Research Award, Ph.D. Forum, IEEE/ACM Design Automation Conference, 2017 (Supervisor for the student)
- Included in the List of Teachers Ranked as Excellent for Fall 2017
- Plenary Speech, IEEE Computer Society Annual Symposium on VLSI, 2018
- Best Paper Award, IEEE/ACM International Workshop on System-Level Interconnect Prediction, 2018
- Third Place Winner, System Design Contest at Design Automation Conference, 2018
- Keynote Speaker, International Conference on Big Data Analytics & Data Mining, 2018
- Judge, 2018 InnovateFPGA Grand Final Competition, Intel, 2018
- Student Innovation Award, IEEE HPEC Graph Challenge, 2018 (Supervisor for the students)
- Boeing Global Technology Student Recognition Award, 2018 (Supervisor for the students)
- Best Poster Award, IBM AI Horizons Colloquium, 2018
- Best Paper Award, IEEE/ACM International Conference on Computer-Aided Design, 2018
- NSF SBIR (Small Business Innovation Research) Phase II Award, with Inspirit IoT, Inc., 2018
- Best Paper Candidate, IEEE/ACM International Symposium on Microarchitecture, 2018
- Invited Special Session Speaker, COOL Chips, 2019
- IEEE Fellow, 2019
- ACM Distinguished Speaker, 2019-2022
- Editor-in-Chief, ACM Transactions on Reconfigurable Technology and Systems, 2019-2022

Research Grants and Contracts

- Research gift, Altera, $20,000, (PI: Chen portion=**$10,000**), 2006
  Title: Novel Logic Synthesis for the New Challenges in FPGAs
- SRC, $360,000, (co-PI, Chen portion=**$180,000**), 2007-2010
  Title: Modeling, Mitigating, and Tolerating Faults due to Parameter Variation in Multicores: A Microarchitecture and CAD Approach
- Research gift, Altera, $15,000, (PI, Chen portion=**$7,500**), 2007
  Title: New Techniques in Synthesis and Physical Design for FPGAs
- NSF, $1,386,000, (co-PI, Chen portion=**$442,000**), 2007-2011

Title: High-performance Reliable Computing: Addressing the Parameter-variation Challenge through a Cross-disciplinary Architecture, CAD, and Compiler Approach

- NSF, **$400,000**, CAREER Grant, Single PI, 2008-2013
  Title: CAREER: Nano-Centric Design Methodology for Nanoscale FPGAs
- Research gift, UIUC research board, $12,000, (co-PI, Chen portion=**$6,000**), 2008
  Title: SOS: A Nanotube-Based Configurable Logic Fabric
- Research gift, Altera, $20,000, (PI, Chen portion=**$10,000**), 2008
  Title: Novel FPGA Synthesis for Low Power
- Research gift, Sun Microsystems, **$23,000**, Single PI, 2008-2010
  Title: Reliable Circuit Design Methodology
- Intel Undergraduate Research Program (ISUR), **$3,200**, Single PI, 2009-2010
- MARCO/DARPA, Gigascale System Research Center, **$236,400**, Single PI, 2009-2012
  Title: Parallel Programming Flow for Efficient FPGA Execution
- Internal gift fund to support PI's research at UIUC, Advanced Digital Sciences Center (ADSC), **$500,000**, Single PI, 2010-2016
  Title: GPU, Reconfigurable Computing, and High-level Synthesis for Application Acceleration
- ADSC/Singapore, **$1.3M**, Grant to support research within ADSC, Single PI, 2010-2013
  Title: Accelerating Immersive Remote Reality Using FPGAs and GPUs
- Research gift, Intel, **$25,000,** Single PI, 2012-2013
  Title: High-Level Synthesis for Accelerator Evaluation and Generation
- UIUC IN^3 (Interdisciplinary Innovation Initiative) fund, Office of the Vice Chancellor for Research/Liberal Arts & Sciences, $200,000, (one of 7 PIs, Chen portion=**$22,000**), 2012-2014
  Title: Developing an Interdisciplinary Research Program in Cancer Genomics
- NSF/SRC, $350,000, (PI, Chen portion = **$175,000**), 2013-2016
  Title: Collaborative Research: From High-level Synthesis to Layout: a Cross-layer Methodology for Large-scale Reliable IC Design
- SRC/DARPA, Center for Future Architectures Research (C_FAR), **$450,000**, co-PI, 2013-2015
  Title: Scalable Synthesis, Exploring Emerging Technologies for Accelerators, and Mapping Diverse Software to Heterogeneous Architectures
- Intel, **$300,000**, Single PI, 2013-2016
  Title: Customized Polyhedral Compilation for Low-Power High-Level SoC Synthesis
- ADSC/Singapore, **$1.4M**, Grant to support research within ADSC, PI, 2013-2016
  Title: Next-Generation Compilers and Architectures for Computation Acceleration with Energy Efficiency
- Research gift, IBM, **$75,000**, Faculty Award, 2014, 2015
  Title: DNA Data Error Correction and Compression with IBM Power8 System
- NSF, **$120,000** as the Graduate Research Fellowship given to a graduate student, 2013-2016
  Title: NSF Graduate Research Fellowship for Research on Hardware Security
- NSF, Research Fellowship for a graduate student (equivalent to one RA support), 2014-2015
  Title: CompGen Fellowship for DNA Error Correction and Genome Mapping
- SRC, $390,000, PI (Chen portion=**$165,000**), 2014-2017
  Title: A New Modular and Global High-level Synthesis Engine for Rapid Post-Silicon Validation of Customized Hardware and Accelerators
- NIH, **$1.3M**, co-PI (one of six), 2015-2018
  Title: Genomic Compression: From Information Theory to Parallel Algorithms
- Research gift, Jump Trading, **$105,000**, Single PI, 2015-2017
  Title: Novel Architecture and Machine Learning Studies
- IBM, C3SR Center, **$900,000,** Co-PI, 2016-2021.
  Title: System and Acceleration for Cognitive Computing and Artificial Intelligence

- NSF and industrial partners, CCBGM Center, **$130,000**, Co-PI, 2017-2020
  Title: Improving Variant Calling through Deep Learning
- Research grant, Boeing, **$80,000,** Single PI, 2017-2018.
  Title: Object Recognition and Tracking for UAVs with Embedded FPGAs and GPUs
- SRC, $210,000, PI (Chen portion=**$120,000**), 2018-2021
  Title: MegaBrain: Enabling Earth-scale FPGA Networks for Cognitive Computing
- ADSC/Singapore, the new CREATE center funded by NRF of Singapore, **$15M**, Co-PI (one of seven), 2017-2022.
  Title: Accelerating Secure Authentication Protocols in the Smart Grid with FPGAs
- DARPA, $4.5M, Co-PI (Chen portion=**$500K**), 2018-2021
  Title: DDARING: Dynamic Data-Aware Reconfiguration, INtegration and Generation
- ZJU-UIUC Research Program, **$75,000**, Single PI, 2018-2019
  Title: Cognitive Computing on Large FPGA Networks
- Research gift, XMotors.ai, **$380,000**, PI (Chen portion=**$145,000**), 2019-2021
  Title: Machine Learning Algorithm Design and Acceleration for Autonomous Driving Cars

Teaching Experiences and Contributions

- Fall 2003/2004, Teaching Assistant, CS 258G: Logic Synthesis of Digital Systems, University of California, Los Angeles
- Spring 2008/2009/2010, ECE 412: Microcomputer Laboratory
- Spring 2006/2007/2009, Fall/2016, ECE 425: Introduction to VLSI System Design. Became the course director in 2019.
- Fall 2006/2007, ECE 598BL: Design and Synthesis of System-on-Chip (new course developed)
- Fall 2008/2009/2010/2011/2013/2015/2017/2018, ECE 527: System-on-Chip Design (permanent version of ECE 598BL above)
- Fall 2011/Spring 2019, ECE 411: Computer Organization and Design (required design course for Computer Engineering majors)
- Fall 2013/Spring 2014, ECE 298: Digital System Design Laboratory (new course developed). This course became the new ECE 385 course in Fall 2014, which is a required course for all ECE undergraduate students.
- Fall 2014, Spring 2012/2013/2016/2017, ECE 385: Digital Systems Laboratory
- Spring 2018, ECE 462: Logic Synthesis
- Spring 2019, ECE 498 ICC: IoT and Cognitive Computing (new course developed)

Hardware Donations

- Equipment grant, Intel, equivalent to $20,000, 2005
- FPGA boards (30 DE2 boards, two DE3 boards, and one DE5 board), Altera, equivalent to $28,000, 2006, 2009, 2013
- TRDB_DC2 1.3Mega Pixel Digital Camera Module (30 items), Altera, equivalent to $2,100, 2006.
- FPGA boards (one Virtex-5 board, 25 Zedboards, and one high-end Virtex-7 board), Xilinx, equivalent to $19,000, 2009, 2013, 2014
- 260 DE2-115 FPGA boards, Altera, equivalent to commercial value of $130,000, to be used in ECE 385, the new course version developed, 2014, 2015, 2016
- Altera Arria 10 board, equivalent to $4,000, 2016.
- Xilinx Virtex UltraScale+ board, equivalent to $6,995, 2017.

- Xilinx, two V7-VC709-G boards, equivalent to $10,000, 2017.
- Xilinx, Zynq UltraScale+ MPSoC ZCU102, equivalent to $2,500, 2018
- Intel, Arria 10 SoC, equivalent to $4,500, 2018

Software Donations and Instruction Grants

- Software donation, Microsoft
- Quartus II design environment and Nios II embedded soft processors (30 licenses), Altera
- Xilinx Vivado Design Suite (50 licenses), Xilinx
- UIUC SIIP (Strategic Instructional Initiatives Program) fund, UIUC College of Engineering, one of 16 PIs, $125,000 for the first year, 2012-2015

Professional Activities, Membership, and Services

Editorship:

- Editor-in-Chief, ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2019- – 2022
- Associate Editor, IEEE Transactions on Circuits and Systems II (TCAS-II), 2016 – present
- Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2013 – present
- Lead Guest Editor, Special Issue of *Integration, the VLSI Journal* on Hardware Acceleration for Machine Learning, 2018-2019
- Guest Editor and main contact, Special Issue of *IEEE Design & Test Magazine* on Machine Intelligence at the Edge, 2018-2019
- Associate Editor, IET Cyber-Physical Systems: Theory & Applications, 2016 – present
- Associate Editor, Journal of Low Power Electronics (JOLPE), 2009 – present
- Associate Editor, Journal of Nanotechnology: Nanomedicine & Nanobiotechnology (NTMB), 2014 – present
- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2012 – 2018
- Associate Editor, ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2017 – 2018 (Guest Associate Editor, 2015-2016)
- Associate Editor, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2009 – 2015
- Associate Editor, IEEE Transactions on Circuits and Systems I (TCAS-I), 2009 – 2012
- Lead Guest Editor for a special issue of Journal of Electrical and Computer Engineering on "ESL Design Methodology", 2011
- Associate Editor, Journal of Circuits, Systems and Computers (JCSC), 2009 – 2012
- Associate Editor, ACM SIGDA Electronic Newsletter, 2008 – 2010
- Associate Editor, VLSI Circuit and Semiconductor Technology Division, Translated Series on Foreign Advanced Technologies, China Machine Press, 2007

Professional Society Membership and Leadership:

- IEEE, member since 2000; IEEE Circuits and Systems Society, and Computer Society
- ACM, member since 2003
- Member, The Design Automation Technical Committee (DATC)
- Member, ACM SIGDA FPGA, Configurable Computing Technical Committee, 2010 – present

- Co-chair, ACM SIGDA Logic/RTL Synthesis Technical Committee, 2010 – 2013

Service to Professional Conferences:

Various chair positions

- Session chair, IEEE International Conference on Computer Design (ICCD), 2005, 2010
- Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2007, 2011, 2014
- Session chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2007-2011, 2017-2018
- Session chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2008, 2010, 2013, 2014
- Session organizer or chair, IEEE/ACM Design Automation Conference (DAC), 2009, 2010, 2014
- Session chair, Design, Automation and Test in Europe (DATE), 2009
- Session chair, IEEE System Level Interconnect Prediction (SLIP), 2009, 2010
- TPC Subcommittee chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2009, 2010, 2011, 2013
- TPC CAD track co-chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- TPC CAD track chair/co-chair, IEEE International Symposium on Circuits and Systems (ISCAS), 2010-2011
- TPC Track chair, IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2011
- TPC Track chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2012
- TPC Track chair, IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2012
- Finance chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2010
- Publications chair, IEEE Symposium on Application Specific Processors (SASP), 2010
- Finance chair, IEEE Symposium on Application Specific Processors (SASP), 2011
- Program chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2011
- CANDE Workshop chair, 2011
- General chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2012
- Program chair, Pacific-Rim Outlook Forum on IC Technology (PROFIT), 2012
- Publicity chair, IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2013-2015
- TPC Track chair, IEEE International Conference on Computer Design (ICCD), 2014-2016
- TPC Track chair, IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2014-2016
- Program chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2015
- General chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2016
- Program co-chair, First International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC), 2015
- Finance chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2017
- Program co-chair, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2017
- Sponsorship chair, IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2017
- General chair, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2018

- General chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2021

Technical program committee member

- ACM/SIGDA International Symposium on FPGA (FPGA), 2006-2019
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2018-2019
- International Conference on Field Programmable Logic and Applications (FPL), 2008-2019
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2007-2011, 2013-2014
- IEEE International Symposium on Circuits and Systems (ISCAS), 2007-2008, 2010-2011
- IEEE International Conference on Computer Design (ICCD), 2007-2016
- IEEE/ACM International Symposium on Quality Electronic Design (ISQED), 2009-2014
- IEEE International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2009-2011
- IEEE Reconfigurable Architectures Workshop (RAW), 2009-2010
- IEEE/ACM Design Automation Conference (DAC), 2009-2011, 2015-2018
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- IEEE Symposium on Application Specific Processors (SASP), 2009
- IEEE/ACM System Level Interconnect Prediction (SLIP), 2009-2012
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2009-2012, 2018
- International Workshop on High-Performance Reconfigurable Computing Technology and Applications (HPRCTA), 2009-2010
- ACM/SIGDA Ph.D. Forum at DAC, 2007-2014
- IEEE International Conference on VLSI Design (VLSI), 2010-2011
- Design, Automation, and Test in Europe (DATE), 2010-2011
- IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2010-2016, 2018
- Workshop on Emerging Parallel Architectures (WEPA), 2011-2012
- International Workshop on Logic and Synthesis (IWLS), 2011
- IEEE International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES), 2013-2014
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2014
- IEEE International Conference on High Performance Computing (HiPC), 2015
- International Workshop on High-performance Reconfigurable Computing (H2RC), 2015
- Steering Committee Member, IEEE/ACM System Level Interconnect Prediction (SLIP), 2014-2019
- International European Conference on Parallel and Distributed Computing (Euro-Par), 2017

Special Session/Workshop/Panel organizer

- Workshop co-organizer and co-coordinator: “Grand Challenges in FPGA Research”, 2007
- Panel chair and moderator: “CMOS vs. NANO: Comrades or Rivals,” ACM/SIGDA International Symposium on FPGA, 2009
- Panel organizer and moderator, "Impact of Emerging Interconnect Technologies on SLIP Research Directions", IEEE/ACM System Level Interconnect Prediction (SLIP), 2009
- ACM/SIGDA 2009 University Booth Keynote Speech organizer and moderator, 2009
- Hot Topic Session co-organizer, “Memristor: Device, Design and Application”, Design, Automation, and Test in Europe (DATE), 2010

- Special session organizer: "ESL Design", IEEE International Conference on ASIC (ASICON), 2011
- Special session organizer: "Would Emerging Technologies Revolutionize How We Achieve Low Power?" IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2013
- Special session organizer: "Energy Efficiency, Complexity, and High-Level Design Methodologies" IEEE International Symposium on Integrated Circuits (ISIC), 2014
- Special session organizer: "Devices, Systems, and Design Methodologies for IoT", IEEE International Conference on ASIC (ASICON), 2015
- Special session organizer: "High-Level Synthesis – Now, the Future, and the Dark Secrets", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2016
- Keynote session co-organizer: "Plenary Session in Memory of Prof. Edward J. McCluskey" IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2017
- Special session organizer: "Where Are the True Innovations and Potentials of IoT?" IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2017
- Special session organizer: "Deep Learning for Applications that Live on Big Data", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018
- Panel chair and moderator: "FPGAs in Supercomputers: Opportunity or Folly?" ACM/SIGDA International Symposium on FPGA (FPGA), 2019

Tutorials, Short Courses, and Panels

- Panelist: "Best ways to Use Billions of Devices on a Chip," IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2008.
- Tutorial presenter: "Latest Advances and Future Opportunities on CAD for FPGAs," IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2008.
- Tutorial organizer and presenter: "From Nanodevices to Nanosystems: Promises and Challenges of IC Design with Nanomaterials," IEEE/ACM Design Automation Conference (DAC), 2009.
- Panelist: Session discussion, IEEE/ACM System Level Interconnect Prediction (SLIP), 2009, 2010.
- Dragon Star Lecture Series, Sichuan University, China, 2011.
- Tutorial organizer and presenter: "The Device-to-System Spectrum – A Tutorial on IC Design with Nanomaterials," Design, Automation & Test in Europe (DATE), 2012.
- Short lectures: "SoC Design Methodology," School of Information Science and Technology, Xiamen University, China, 2012.
- Tutorial co-organizer and presenter: "High-Level Synthesis for Low-Power Design," IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2014.
- Tutorial instructor: "Bloom-filter Based DNA Error Correction and Acceleration Using FPGAs," Workshop on Genome Assembly and Annotation, Bio IT World Conference & Expo, Boston, 2014.
- Panelist: Bio-informatics session of the CSL Student Conference of UIUC, Feb. 2017.
- Short course: "Recent Advances of High-level Synthesis", ShanghaiTech University, July 2017.
- Week-long short course: "Digital Design with FPGAs", Training course for engineers of Jump Trading, August 2017 and December 2017.
- Panelist: "The Future of AI", SingularityU Warsaw Chapter Conference, 2017.
- Panelist: "AI Chip", SV Connect Conference, 2017.
- Tutorial presenter: "Accelerating Deep Neural Networks on FPGAs", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018.

Proposal Review

- External proposal reviewer, Natural Sciences and Engineering, Research Council of Canada, 2008, 2009, 2010
- External proposal reviewer, Israel Science Foundation, 2008
- External research proposal reviewer, Qatar National Research Fund, 2009, 2011, 2012, 2014
- External research proposal reviewer, Nanyan Technology University, Singapore, 2010
- NSF panelist, Computing and Communications Foundations Division, 2012
- NSF panelist, Computing and Communications Foundations Division, 2012
- External proposal reviewer, Intramural Discovery Grant Program, Vanderbilt University, 2013
- Proposal reviewer for U. S. Army Research Office, 2014
- NSF panelist, CISE, 2015, 2016, 2019

Journal Review

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Advanced Packaging (TAP)
- ACM Transactions on Reconfigurable Technology and Systems (TRETS)
- IEEE Transactions on Nanotechnology (TN)
- Integration, the VLSI Journal
- Journal of Low Power Electronics (JOLPE)
- IET Circuits, Devices & Systems
- IEEE Design & Test of Computers
- IEEE Transactions on Industrial Informatics
- Applied Physics A
- ACM Transactions on Architecture and Code Optimization (TACO)
- IEEE Transactions on Cyber-Physical Systems (TCPS)
- Briefings in Bioinformatics
- IEEE Transactions on Circuits and Systems for Video Technology

Student and Postdoc Advising

Current Graduate Students:

(*Ph.D. Candidate* indicates that the student has passed either the Ph.D. qualifying exam or the Ph.D. prelim exam**)**

- Ashutosh Dhar (Ph.D. Candidate)
- Di He (Ph.D. Candidate)
- Sitao Huang (Ph.D. Candidate), co-advised with Prof. Wen-Mei Hwu
- Dae Hee Kim
- Gregory Knox
- Qin Li
- Yuhong Li
- Yi Liang (Ph.D. Candidate)
- Jong Bin Lim (Ph.D. Candidate)

- Xinheng Liu (Ph.D. Candidate)
- Yujia Qiu
- Anand Ramachandran (Ph.D. Candidate)
- Wei Ren
- Kenny Umenthum
- Vibhakar Vemulapati
- Mang Yu
- Xiaofan Zhang (Ph.D. Candidate)
- Xingkai Zhou
- Wei Zuo (Ph.D. Candidate)

Current Postdoc Researchers:

- Cong Hao

Current Undergraduate Researchers:

- Keshav Harisrikanth
- Paul Jeong
- Jack Li
- Ximin Lin
- Junhao Pan

Current Research Group Members within ADSC (Illinois Center in Singapore):

- Yao Chen (Postdoc researcher)
- Kai Zhang (Software engineer)

Alumni from UIUC:

- Lei Cheng, Ph.D., 2007 (co-advised with Prof. Martin Wong; joined Synplicity)
- Shoaib Akram, M.S., 2009 (joined Institute of Computer Science, Foundation for Research and Technology, Greece)
- Scott Cromar, M.S., 2009 (joined law school, UIUC)
- Scott Chilstedt, M.S., 2010 (joined IBM)
- Greg Lucas, M.S., 2010 (joined Intel)
- Chi-Chen Peng, M.S., 2010 (joined Springsoft; now Synopsys)
- Chen Dong, Ph.D., 2010 (joined Magma; now Synopsys)
- Artem Rogachev, M.S., 2012 (joined TI)
- Lu Wan, Ph.D., 2012 (joined Tensilica; now Cadence)
- Alex Papakonstantinou, Ph.D., 2012 (joined NVidia)
- Jacob Tolar, M.S., 2013 (joined Yahoo)
- Chong Li, M.S., 2013 (joined University of Washington as a Ph.D. student)
- Amit Sangai, M.S., 2013 (joined law school, India)
- Chunan Wei, M.S., 2014 (joined Qualcomm)
- Ying Chen, M.S., 2015 (joined Google)
- Pranay Vissa, M.S., 2015 (joined a startup in silicon valley)
- Yun Heo, Ph.D., 2015 (joined Samsung)

- Ying-Yu Chen, Ph.D., 2015 (joined Synopsys)
- Warren Kemmerer, M.S., 2016 (joined Intel)
- Yan Yan, M.S., 2016 (joined Google)
- Zelei Sun, M.S., 2016 (joined Google)
- Sven Choden Konigsmark, Ph.D., 2017 (co-advised with Prof. Martin Wong; joined Google)
- Daniel Chen, M.S., 2017 (joined a startup in silicon valley)
- Gowthami Manikandan, M.S., 2017 (joined Apple)
- Keith Campbell, Ph.D., 2017 (joined Inspirit IoT)
- Chuanhao Zhuge, M.S., 2017 (joined Apple)
- Chen-Hsuan Lin, Ph.D., 2018 (joined Google)
- Zhangqi Xu, M.S., 2018 (joined a startup in silicon valley)
- Huiren Li, M.S., 2018 (joined Amazon)

- **Undergraduate Researchers:**
  Bryan Clodfelter, Jaeho Lee, Kyungmin Lee, Allyson Moisan, Andrew Ryan, Alexander Uribe, Yohannes Kifle, Christine Lee, Wenxun Huang, Artem Rogachev, Shuotao Xu, Sai Ma, Chunan Wei, Tielong Su, Liana Nicklaus, Daniel Chen, Chuanhao Zhuge, Xinheng Liu, George Li, Huiren Li, Dae Hee Kim, Kenny Umenthum, Luis Pabon, Wei-You Chen, Leon He, Nitesh Neupane, Zizhen Liu, Yikuan Chen, Qin Li, Yujia Qiu, Mang Yu, Yangyang Yu, etc.
  Many of them are either in top graduate schools (such as MIT, Berkeley, Harvard, and UIUC) or in high-tech companies (such as Microsoft, ARM, and TI) now.

Alumni from ADSC:

- Dr. Eric (Yun) Liang, postdoc researcher (Research Scientist) of ADSC (2010-2012), now associate professor of Peking University, China
- Dr. Gabriel Noaje, postdoc researcher (Research Scientist) of ADSC (2013-2014), now Senior Computational Scientist at A*STAR Computational Resource Centre, Singapore
- Dr. Swathi Gurumani, postdoc researcher (Principal Research Engineer) of ADSC (2012-2016), visiting faculty of IIIT, India in 2016, now VP of Engineering of Inspirit IoT, Inc.
- Dr. Kyle Rupnow, postdoc researcher (Senior Scientist) of ADSC (2010-2016), assistant professor of NTU, Singapore (2012-2015), now CTO of Inspirit IoT, Inc.
- Mr. Tan Nguyen, software engineer of ADSC, now Ph.D. student of UC Berkeley
- Dr. Liwei Yang, senior software engineer of ADSC, now Scientist at Institute of High Performance Computing, Singapore
- Ms. Zheng Cui, software engineer of ADSC, now at Ubisoft Singapore
- Dr. Hongbin Zheng, senior software engineer of ADSC, now at Amazon AWS
- Mr. Muhammad T. Satria, software engineer of ADSC, now at JPMorgan Chase & Co.

Research Interests

- System-level and high-level synthesis
- FPGA and reconfigurable computing
- Cognitive computing and machine learning
- GPU optimization and GPU computing
- Hardware/software co-design for SoCs or heterogeneous computing systems
- Computational genomics
- Hardware security

News Articles

Chen Named as Next Editor-in-Chief of ACM TRETS
https://ece.illinois.edu/newsroom/article/29157

Chen and Choudhury Elevated as IEEE Fellows
https://ece.illinois.edu/newsroom/article/29123

Chen's Inspirit IoT Startup Awarded Phase II NSF SBIR Grant
https://www.prnewswire.com/news-releases/inspirit-iot-awarded-phase-ii-nsf-sbir-grant-to-support-development-of-dnn-architect-300720038.html

ECE Illinois Researchers Pursue World Class Computing and Programmability Through DARDA Project
https://ece.illinois.edu/newsroom/article/27542

Chen's Inspirit IoT Startup Making Waves in Industry, Academia
https://csl.illinois.edu/news/chen%E2%80%99s-inspirit-iot-startup-making-waves-industry-academia

Wired In: Deming Chen | News-Gazette.com
http://www.news-gazette.com/news/business/2017-09-17/wired-deming-chen.html

LOW-COST AUDIO SECURITY SYSTEM HELPS RESEARCHERS WIN IEEE COMPETITION
https://ece.illinois.edu/newsroom/article/23447

Illinois, start-up researchers win DAC-IoT competition with low-cost audio security system
https://csl.illinois.edu/news/illinois-start-researchers-win-dac-iot-competition-low-cost-audio-security-system

ICCAD Best Paper Award
https://www.ece.illinois.edu/newsroom/article/15131

Chen and Li Named 2015 Willett Scholars
http://www.ece.illinois.edu/newsroom/article/11139

Faculty receive IBM recognition, funding for research contributions
http://csl.illinois.edu/news/faculty-receive-ibm-recognition-funding-research-contributions

Researchers Release First SPICE-compatible Compact Models for Graphene-based Digital Circuits
http://csl.illinois.edu/news/researchers-release-first-spice-compatible-compact-models-graphene-based-digital-circuits

High-level Synthesis on Fire: Research Receives Recognition from Academia, Industry
http://www.ece.illinois.edu/mediacenter/article.asp?id=6013

ECE Receives Zedboard Donation for Research, Education
http://www.ece.illinois.edu/mediacenter/article.asp?id=7389

Chen Receives Intel Gift to Study Increasing Computer Performance and Efficiency
http://www.ece.illinois.edu/mediacenter/article.asp?id=1686

ECE Faculty and Students Win IEEE FCCM Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=1270

Chen and Hwu Win IEEE SASP'09 Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=512

Chen Promotes Nanotechnology Research
http://www.ece.illinois.edu/mediacenter/article.asp?id=182

Graduate Students and Professor Team Up to Win Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=181

ECE Faculty Receive CAREER Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=176

Illinois Named an OpenSPARC Center of Excellence
http://www.ece.illinois.edu/mediacenter/article.asp?id=366

Publications

Books

[1] N. Jha and D. Chen, editors, *Nanoelectronic Circuit Design*, Springer Publishers. 2011.

Book Chapters

[1] D. Chen, "Chapter 38: Design Automation for Microelectronics," *Handbook of Automation*, Springer Publishers, 2009.

[2] S. Chilstedt, C. Dong, and D. Chen, "Carbon Nanomaterial Transistors and Circuits," *Transistors: Types, Materials, and Applications*, Nova Science Publishers, 2010.

[3] C. Dong, S. Chilstedt, and D. Chen, "FPCNA: a Carbon Nanotube-Based Programmable Architecture," *Nanoelectronic Circuit Design*, Springer Publishers, 2011.

[4] W. Zuo, S. Gurumani, K. Rupnow, and D. Chen, "New Solutions for Cross-Layer System-Level and High-Level Synthesis," *Emerging Technology and Architecture for Big-data Analytics*, Springer Publishers, 2017.

Monographs

[1] D. Chen, J. Cong, and P. Pan, FPGA Design Automation: A Survey, Foundations and Trends in Electronic Design Automation, NOW Publishers, 137 pages, November 2006.

Journal Papers

[1] D. Chen, J. Cong, M. Ercegovac, and Z. Huang, "Performance-Driven Mapping for CPLD Architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 22, No. 10, pp. 1424-1431, October 2003.

[2] F. Li, Y. Lin, L. He, D. Chen, and J. Cong, "Power Modeling and Characteristics of Field Programmable Gate Arrays," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, Issue 11, pp. 1712-1724, November 2005.

[3] D. Chen, J. Cong, and J. Xu, "Optimal Simultaneous Module and Multi-Voltage Assignment for Low-Power," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 11, Issue 2, pp. 362-386, April 2006.

[4] C. Dong, D. Chen, S. Haruehanroengra, and W. Wang, "3-D nFPGA: A Reconfigurable Architecture for 3-D CMOS/Nanomaterial Hybrid Digital Circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 54, Issue 11, pp. 2489-2501, November 2007.

[5] L. Cheng, D. Chen, and D.F. Wong, "A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 13, No. 2, Article 34, pp. 1-15, April 2008.

[6] L. Cheng, D. Chen, and D.F. Wong, "DDBDD: Delay-Driven BDD Synthesis for FPGAs", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 27, No. 7, pp.1203-1213, July 2008.

[7] S. Chilstedt, C. Dong, and D. Chen, "Design and Evaluation of a Carbon Nanotube-Based Programmable Architecture", *International Journal of Parallel Programming (IJPP), Special Issue on Nano/Bio-Inspired Applications, Architectures and Software*, Vol. 37, Issue 4, pp. 389-416, August 2009.

[8] H. Li, D. H. Kwon, D. Chen, and Y. Chiu, "A Fast Digital Predistortion Algorithm for Radio-Frequency Power Amplifier Linearization with Loop Delay Compensation," *IEEE Journal of Selected Topics in Signal Processing, Special Issue on: DSP Techniques for RF/Analog Circuit Impairments*, Vol. 3, No. 3, pp.374-383, June 2009.

[9] D. Chen and S. Cromar, "An Optimal Resource Binding Algorithm with Inter-Transition Switching Activities for Low Power", *Journal of Low Power Electronics*, Vol. 5, No. 4, pp. 454-463, December 2009.

[10] Q. Dinh, D. Chen, and D. F. Wong, "A Routing Approach to Reduce Glitches in Low Power FPGAs", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 29, Issue 2, pp. 235-240, February 2010.

[11] D. Chen, J. Cong, Y. Fan, and L. Wan, "LOPASS: A Low-Power Architectural Synthesis System for FPGAs with Interconnect Estimation and Optimization", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 18, No. 4, pp. 564-577, April 2010.

[12] S. Akram, A. Papakonstantinou, R. Kumar, and D. Chen, "Workload Adaptive Shared Memory Multicore Processors with Reconfigurable Interconnects," *Journal of Reconfigurable Computing*, Vol. 2010, Article ID 205852, 22 pages, 2010.

[13] D. Chen, J. Cong, C. Dong, L. He, F. Li, and C. Peng, "Technology Mapping and Clustering for FPGA Architectures with Dual Supply Voltages," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 29, No. 11, pp. 1709-1722, Nov. 2010.

[14] G. Lucas, C. Dong, and D. Chen, "Variation-Aware Placement with Multi-cycle Statistical Timing Analysis for FPGAs", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 29, No. 11, pp. 1818-1822, Nov. 2010.

[15] L. Wan and D. Chen, "Analysis of Digital Circuit Dynamic Behavior with Timed Ternary Decision Diagrams for Better-Than-Worst-Case Design", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 31, No. 5, pp. 662-675, May 2012.

[16] Y. Liang, K. Rupnow, Y. Li, D. Min, M. Do, and D. Chen, "High Level Synthesis: Productivity, Performance and Software Constraints", *Journal of Electrical and Computer Engineering, Special Issue on ESL Design Methodology*. Volume 2012, Article ID 649057, 14 pages, 2012.

[17] L. Wan, C. Dong and D. Chen, "A Coarse-Grained Reconfigurable Architecture with Compilation for High Performance," *International Journal of Reconfigurable Computing, Special Issue on High Performance Reconfigurable Computing.* Volume 2012, Article ID 163542, 17 pages, 2012.

[18] X-L. Wu, Y. Heo, I. El Hajj, W-M. Hwu, D. Chen, and J. Ma, "TIGER: Tiled Iterative Genome Assembler," *BMC Bioinformatics*, 2012, **13**(Suppl 19):S18, December 2012.

[19] A. Papakonstantinou, K. Gururaj, J. Stratton, D. Chen, J. Cong, and W.M. Hwu, "Efficient Compilation of CUDA Kernels for High-Performance Computing on FPGAs," *ACM Transactions on Embedded Computing Systems*. Vol. 13, Issue 2, September 2013.

[20] T. Yan, Q. Ma, S. Chilstedt, M. D.F. Wong, and D. Chen, "A Routing Algorithm for Graphene Nanoribbon Circuit," *ACM Transactions on Design Automation of Electronic Systems - Special Section on Networks on Chip: Architecture, Tools, and Methodologies*, Vol. 18, Issue 4, October 2013.

[21] Y. Heo, X-L. Wu, D. Chen, J. Ma, and W-M Hwu, "BLESS: Bloom-filter-based Error Correction Solution for High throughput Sequencing Reads," *Bioinformatics*, doi: 10.1093/bioinformatics /btu030, January 2014.

[22] H. Luo, S. Wei, D. Chen, and D. Guo, "Hybrid Circuit-Switched Network for On-Chip Communication in Large-Scale Chip-Multiprocessors," *Journal of Parallel and Distributed Computing*, Vol 74, Issue 9, pp. 2818-2830, September 2014.

[23] M. Gholipour, N. Masoumi, Y-Y. Chen, D. Chen, and M. Pourfath, "Asymmetric Gate Schottky-Barrier Graphene Nano-Ribbon FETs for Low Power Design," *IEEE Transactions on Electron Devices*, Vol. 61, No. 12, December 2014.

[24] H. Zheng, S. T. Gurumani, L. Yang, D. Chen, and K. Rupnow, "High-level Synthesis with Behavioral-level Multi-cycle Path Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol 33, No. 12, pp 1832-1845, December 2014.

[25] Z. Zhang, D. Chen, S. Dai, and K. Campbell, "High-Level Synthesis for Low-Power Design," *IPSJ Transactions on System LSI Design Methodology*, Vol. 8 (2015) pp. 12-25, February 2015.

[26] Y. Liang, H. P. Huynh, K. Rupnow, S. M. Goh, and D. Chen, "Efficient GPU Spatial-Temporal Multitasking," *IEEE Transactions on Parallel and Distributed Systems*, Vol 26, Issue 3, pp. 748-760, March 2015.

[27] M. Gholipour, Y.Y. Chen, A. Sangai, N. Masoumi, and D. Chen, "Analytical SPICE-Compatible Model of Schottky-Barrier-Type GNRFETs with Performance Analysis", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, March 2015.

[28] N. Liu, H. Li, H. Dai, D. Guo, and D. Chen, "Robust Blind Image Watermarking Based on Chaotic Mixtures", *Nonlinear Dynamics*, Vol 80, Issue 3, pp. 1329-1355, May 2015.

[29] X. Xie, Y. Liang, G. Sun, and D. Chen, "An Efficient Compiler Framework for Cache Bypassing on GPUs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 34, No. 10, pp. 1677-1690, October 2015.

[30] Y.Y. Chen, A. Sangai, A. Rogachev, M. Gholipour, G. Iannaccone, G. Fiori, and D. Chen, "A SPICE-Compatible Model of MOS-Type Graphene Nano-ribbon Field-Effect Transistors enabling

Gate- and Circuit-level Delay and Power Analysis under Process Variation," *IEEE Transactions on Nanotechnology*, Volume 14, Issue 6, pp. 1068-1082, November 2015.

[31] Yun Heo, Anand Ramachandran, Wen-Mei Hwu, Jian Ma, Deming Chen, "BLESS 2: Accurate, memory-efficient, and fast error correction method," *Bioinformatics*, doi: 10.1093/bioinformatics/btw146, 2016.

[32] C. Konigsmark, D. F. Wong, and D. Chen, "PolyPUF: Physically Secure Self-Divergence," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1053-1066, Volume 35, Issue 7, July 2016.

[33] Y. Wu, J. Zhao, D. Chen, and D. Guo, "Modeling of Gaussian Network-Based Reconfigurable Network-on-Chip Designs", *IEEE Transactions on Computers*, pp. 2134-2142, Volume 65, Issue 7, July 2016.

[34] Y. Liang, M. T. Satria, K. Rupnow, and D. Chen, "An Accurate GPU Performance Model for Effective Control Flow Divergence Optimization", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1165-1178, Volume: 35, Issue: 7, July 2016.

[35] Y. Chen, S. T. Gurumani, Y. Liang, G. Li, D. Guo, K. Rupnow, and D. Chen, "FCUDA-NoC: A Scalable and Efficient Network-on-Chip Implementation for the CUDA-to-FPGA Flow", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 2220-2233, Volume: 24, Issue: 6, June 2016.

[36] Y. Chen, T. Nguyen, Y. Chen, S. T. Gurumani, Y. Liang, K. Rupnow, J. Cong, W.M. Hwu, and D. Chen, "FCUDA-HB: Hierarchical and Scalable Bus Architecture Generation on FPGAs with the FCUDA Flow," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 2032-2045, Volume: 35, Issue: 12, 2016.

[37] Deming Chen, Jason Cong, Swathi Gurumani, Wen-mei Hwu, Kyle Rupnow, and Zhiru Zhang, "Platform Choices and Design Demands for IoT Platforms: Cost, Power and Performance Tradeoffs", *IET Cyber-Physical Systems: Theory & Applications*, pp. 70–77, Vol. 1, Iss. 1, November 2016.

[38] K. Campbell, W. Zuo, and D. Chen, "New Advances of High-Level Synthesis for Efficient and Reliable Hardware Design", *Integration, the VLSI Journal*, Volume 58, Pages 189-214, June 2017. **Invited Keynote Paper**.

[39] Nam Sung Kim, Deming Chen, Jinjun Xiong, and Wen-mei Hwu, "Heterogeneous Computing Meets Near-Memory Acceleration and High-level Synthesis in the Post-Moore Era", *IEEE Micro*, pp. 10-18, Volume: 37, Issue: 4, August 2017.

[40] Chen-Hsuan Lin, Wan Lu, and Deming Chen, "C-Mine: Data Mining of Logic Common Cases for Improved Timing Error Resilience with Energy Efficiency," *ACM Transactions on Design Automation of Electronic Systems*, Volume 23, Issue 2, January 2018.

[41] M. Gholipour, Y.Y. Chen, and D. Chen, "Compact Modeling to Device- and Circuit-Level Evaluation of Flexible TMD Field-Effect Transistors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Volume: 37, Issue: 4, Page(s): 820 - 831, April 2018.

[42] Di He, Boon Pang Lim, Xuesong Yang, Mark Hasegawa-Johnson, and Deming Chen, "Acoustic landmarks contain more information about the phone string than other frames for automatic speech recognition with deep neural network acoustic model", *The Journal of the Acoustical Society of America* 143, 3207 (2018); doi: 10.1121/1.5039837.

[43] K. Campbell, D. Lin, L. He, L. Yang, S. Gurumani, K. Rupnow, S. Mitra, and D. Chen, "Hybrid Quick Error Detection: Validation and Debug of SoCs through High-Level Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. To appear.

[44] Keith Campbell, Chen-Hsuan Lin, and Deming Chen, "Cost-Effective Error Detection through Mersenne Modulo Shadow Datapaths," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. To appear.

[45] Subho Banerjee, Mohamed El-Hadedy, Jong Bin Lim, Zbigniew Kalbarczyk, Deming Chen, Steve Lumetta, and Ravishankar Iyer, "ASAP: Accelerated Short-Read Alignment on Programmable Hardware," *IEEE Transactions on Computers*. To appear.

[46] Jianwei Zheng, Chao Lu, Jiefeng Guo, Deming Chen, and Donghui Guo, "A Hardware-Efficient Block Matching Algorithm and Its Hardware Design for Variable Block Size Motion Estimation in Ultra-High-Definition Video Encoding", *ACM Transactions on Design Automation of Electronic Systems*. To Appear.

Conference Papers

[1] D. Chen, R. Colwell, H. Gelman, P. K. Chrysanthis, and D. Mosse, "A Framework for Experimenting with QoS for Multimedia Services," *Proceedings of International Conference on Multimedia Computing and Networking*, pp. 186-197, January 1996. (Acceptance ratio not available)

[2] D. Chen, J. Cong, M. Ercegovac, and Z. Huang, "Performance-Driven Mapping for CPLD Architectures," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 39-47, February 2001. (Acceptance ratio 43%)

[3] F. Li, D. Chen, L. He, and J. Cong, "Architecture Evaluation for Power-Efficient FPGAs," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 175-184, February 2003. (Acceptance ratio 29%)

[4] D. Chen, J. Cong, and Y. Fan, "Low-Power High-Level Synthesis for FPGA Architectures," *Proceedings of IEEE/ACM International Symposium on Low Power Electronics and Design*, pp. 134-139, August 2003. (Acceptance ratio 41%)

[5] D. Chen, J. Cong, F. Li, and L. He, "Low-Power Technology Mapping for FPGA Architectures with Dual Supply Voltages," *Proceedings of ACM International Symposium on Field-Programmable Gate Arrays*, pp. 109-117, February 2004. (Acceptance ratio 27%)

[6] D. Chen and J. Cong, "Register Binding and Port Assignment for Multiplexer Optimization," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 68-73, January 2004. (Acceptance ratio 50%, full paper acceptance ratio 34%)

[7] D. Chen and J. Cong, "Delay Optimal Low-Power Circuit Clustering for FPGAs with Dual Supply Voltages," *Proceedings of IEEE/ACM International Symposium on Low Power Electronics and Design*, pp. 70-73, August 2004. (Acceptance ratio 34%)

[8] D. Chen and J. Cong, "DAOmap: A Depth-Optimal Area Optimization Mapping Algorithm for FPGA Designs," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, pp. 752-759, November 2004. (Acceptance ratio 24%)

[9] D. Chen, J. Cong, and J. Xu, "Optimal Module and Voltage Assignment for Low-Power," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 850-855, January 2005. (Acceptance ratio 40%, full paper acceptance ratio: 14%)

[10] D. Chen, J. Cong, Y. Fan, G. Han, W. Jiang, and Z. Zhang, "xPilot: A Platform-Based Behavioral Synthesis System," *Proceedings of SRC Techcon Conference*, October 2005. (Acceptance ratio not available)

[11] L. Cheng, L. Deng, D. Chen, and D.F. Wong, "A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 117-120, July 2006. (Acceptance ratio 24%)

[12] J. Lin, D. Chen, and J. Cong, "Optimal Simultaneous Mapping and Clustering for FPGA Delay Optimization," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 472-477, July 2006. (Acceptance ratio 24%)

[13] D. Chen, J. Cong, Y. Fan, and J. Xu, "Optimality Study of Resource Binding with Multi-Vdds," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 580-585, July 2006. (Acceptance ratio 24%)

[14] D. Chen, J. Cong, Y. Fan and Z. Zhang, "High-Level Power Estimation and Low-Power Design Space Exploration for FPGAs," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 529-534, Jan. 2007. (Acceptance ratio 32%)

[15] L. Cheng, D. Chen, and D.F. Wong, "DDBDD: Delay-Driven BDD Synthesis for FPGAs," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 910-915, June 2007. (Acceptance ratio 23%)

[16] L. Cheng, D. Chen, and D.F. Wong, "GlitchMap: An FPGA Technology Mapper for Low Power Considering Glitches," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 318-323, June 2007. (Acceptance ratio 23%)

[17] L. Cheng, D. Chen, D.F. Wong, M. Hutton, and J. Govig, "Timing Constraint-driven Technology Mapping for FPGAs Considering False Paths and Multi-Clock Domains," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, pp. 370-375, Nov. 2007. (Acceptance ratio 27%)

[18] C. Dong, D. Chen, S. Haruehanroengra, and W. Wang, "Performance and Power Evaluation of a 3D CMOS/Nanomaterial Reconfigurable Architecture," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, pp. 758-764, Nov. 2007. (Acceptance ratio 27%)

[19] Q. Dinh, Y. Bresler, and D. Chen, "Hardware Acceleration for Sparse Fourier Image Reconstruction," *Proceedings of IEEE International Conference on ASIC*, pp. 1346-1351, Oct. 2007. (**Invited**) (Acceptance ratio not available)

[20] S. Akram, S. Cromar, G. Lucas, A. Papakonstantinou, and D. Chen, "VEBoC: Variation and Error-Aware Design for Billions of Devices on a Chip," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 803-808, January 2008. (**Invited**) (Acceptance ratio 35%)

[21] Q. Dinh, D. Chen, and D.F. Wong, "Efficient ASIP Design for Configurable Processors with Fine-Grained Resource Sharing," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 99-106, February 2008. (Acceptance ratio 30%)

[22] A. Papakonstantinou, D. Chen, and W.M. Hwu, "Application Acceleration with the Explicitly Parallel Operations System - the EPOS Processor," *Proceedings of IEEE Symposium on Application Specific Processors*, pp. 20-25, 2008. (Acceptance ratio 29%)

[23] A. Papakonstantinou, Y. Kifle, G. Lucas, and D. Chen, "MP3 Decoding on FPGA: A Case Study for Floating Point Acceleration," *Proceedings of Reconfigurable Systems Summer Institute*, Urbana, IL, 2008. (Acceptance ratio not available)

[24] G. Lucas, S. Cromar, and D. Chen, "FastYield: Variation-Aware, Layout-Driven Simultaneous Binding and Module Selection for Performance Yield Optimization," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 61-66, January 2009. (**Best Paper Award**) (Acceptance ratio 33%)

[25] B. Greskamp, L. Wan, R. Karpuzcu, J. Cook, J. Torrellas, D. Chen, and C. Zilles, "BlueShift: Designing Processors for Timing Speculation from the Ground Up," *Proceedings of International Symposium on High-Performance Computer Architecture*, pp. 213-224, February 2009. (Acceptance ratio 19%)

[26] C. Dong, S. Chilstedt, and D. Chen, "FPCNA: Field Programmable Carbon Nanotube Array," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 161-170, February 2009. (Acceptance ratio 26%)

[27] Q. Dinh, D. Chen, and D.F. Wong, "A Routing Approach to Reduce Glitches in Low Power FPGAs," *Proceedings of ACM International Symposium on Physical Design*, pp. 99-106, March 2009. (Acceptance ratio 33%)

[28] C. Dong, S. Chilstedt, and D. Chen, "Reconfigurable Circuit Design with Nanomaterials," *Proceedings of Design, Automation and Test in Europe*, pp. 442-447, April 2009. (**Invited**) (Acceptance ratio 23%)

[29] C. Dong, S. Chilstedt, and D. Chen, "Variation Aware Routing for Three-Dimensional FPGAs," *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, pp. 298-303, May 2009. (Acceptance ratio 25%)

[30] S. Cromar, J. Lee, and D. Chen, "FPGA-Targeted High-Level Binding Algorithm for Power and Area Reduction with Glitch-Estimation," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 838-843, July 2009. (Acceptance ratio 22%)

[31] A. Papakonstantinou, K. Gururaj, J. Stratton, D. Chen, J. Cong, and W.M. Hwu, "FCUDA: Enabling Efficient Compilation of CUDA Kernels onto FPGAs," *Proceedings of IEEE Symposium on Application Specific Processors*, pp. 35-42, July 2009. (**Best Paper Award**) (Acceptance ratio 30%)

[32] S. Akram, R. Kumar, and D. Chen, "Workload Adaptive Shared Memory Multicore Processors with Reconfigurable Interconnects," *Proceedings of IEEE Symposium on Application Specific Processors*, pp. 7-14, July 2009. (Acceptance ratio 30%)

[33] L. Wan, C. Dong, and D. Chen, "A New Coarse-Grained Reconfigurable Architecture with Fast Data Relay and Its Compilation Flow," *Proceedings of Symposium on Application Accelerators in HPC*, July 2009. (Acceptance ratio not available)

[34] C. He, A. Papakonstantinou, and D. Chen, "A Novel SoC Architecture on FPGA for Ultra Fast Face Detection," *Proceedings of IEEE International Conference on Computer Design*, pp. 412-418, Oct. 2009. (Acceptance ratio 35%)

[35] L. Wan and D. Chen, "DynaTune: Circuit-Level Optimization for Timing Speculation Considering Dynamic Path Behavior," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, pp. 172-179, Nov. 2009. (Acceptance ratio 26%)

[36] Q. Dinh, D.F. Wong, and D. Chen, "Dynamic Power Estimation for Deep Submicron Circuits with Process Variation," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 587-592, January 2010. (Acceptance ratio 33%)

[37] G. Lucas, C. Dong, and D. Chen, "Variation-Aware Placement for FPGAs with Multi-cycle Statistical Timing Analysis," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 177-180, February 2010. (Acceptance ratio 25%)

[38] Y. Chen, C. Dong, and D. Chen, "Clock Tree Synthesis under Aggressive Buffer Insertion," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 86-89, June 2010. (Acceptance ratio 24%)

[39] Q. Dinh, D. Chen, and D.F. Wong, “BDD-Based Circuit Restructuring for Reducing Dynamic Power,” *Proceedings of IEEE International Conference on Computer Design*, October 2010. (Acceptance ratio 29%)

[40] L. Wan and D. Chen, "Analysis of Circuit Dynamic Behavior with Timed Ternary Decision Diagram," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2010. (Acceptance ratio 30%)

[41] G. Lucas and D. Chen, "Variation-Aware Layout-Driven Scheduling for Performance Yield Optimization," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2010. (Acceptance ratio 30%)

[42] T. Yan, Q. Ma, S. Chilstedt, D.F. Wong, and D. Chen, “Routing with Graphene Nanoribbons,” *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2011. (Acceptance ratio 35%)

[43] C. Peng, C. Dong, and D. Chen, “SETmap: A Soft Error Tolerant Mapping Algorithm for FPGA Designs with Low Power,” *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2011. (Acceptance ratio 35%)

[44] A. Papakonstantinou, Y. Liang, J. Stratton, K. Gururaj, D. Chen, W.M. Hwu and J. Cong, "Multilevel Granularity Parallelism Synthesis on FPGAs," *Proceedings of IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2011. (**Best Paper Award**) (Acceptance ratio 17% for long presentation)

[45] C. Dong, C. Chen, S. Mitra, and D. Chen, "Architecture and Performance Evaluation of 3D CMOS-NEM FPGA," *Proceedings of IEEE/ACM International Workshop on System Level Interconnect Prediction*, June 2011. (Acceptance ratio 35% for long presentation)

[46] S. Liu, A. Papakonstantinou, H. Wang, and D. Chen, "Real-time Object Tracking System on FPGAs," *Proceedings of Symposium on Application Accelerators in High Performance Computing*, July 2011. (**Best Paper Award**)

[47] A. Papakonstantinou, D. Chen, and W.M. Hwu, "A Code Optimization Framework for Performance Portability of Parallel Kernels across GPUs and Custom Accelerators", *SRC Technical Conference (TECHCON)*, Sept. 2011.

[48] A. Rogachev, L. Wan and D. Chen, "Temperature Aware Statistical Static Timing Analysis," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2011. (Acceptance ratio 30%)

[49] K. Rupnow, Y. Liang, Y. Li, and D. Chen, “A Study of High-Level Synthesis: Promises and Challenges”, *IEEE International Conference on ASIC*, October 2011. (**Invited**)

[50] K. Rupnow, Y. Liang, Y. Li, D. Min, M. Do, and D. Chen, “High Level Synthesis of Stereo Matching: Productivity, Performance, and Software Constraints”, *IEEE International Conference on Field-Programmable Technology*, December 2011. (Acceptance ratio 29%) (**Best Paper Nomination**)

[51] Y. Liang, Z. Cui, S. Zhao, K. Rupnow, Y. Zhang, D. L. Jones, and D. Chen, "Real-time Implementation and Performance Optimization of 3D Sound Localization on GPUs", *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2012. (Acceptance ratio 21%)

[52] K. S. Yim, V. Sidea, Z. Kalbarczyk, D. Chen, and R. K. Iyer, “A Fault-Tolerant Programmable Voter for Software-Based N-Modular Redundancy,” *Proceedings of the IEEE Aerospace Conference*, March 2012.

[53] Z. Cui, Y. Liang, K. Rupnow, and D. Chen, "An Accurate GPU Performance Model for Effective Control Flow Divergence Optimization", *Proceedings of IEEE International Parallel & Distributed Processing Symposium*, May 2012. (Acceptance ratio 21%)

[54] W. Huang, Y. Quan, and D. Chen, "Improving Broadcast Efficiency in Wireless Sensor Network Time Synchronization Protocols," *Proceedings of IEEE/ACM International Workshop on System Level Interconnect Prediction*, June 2012.

[55] S. Zhao, S. Ahmed, Y. Liang, K. Rupnow, D. Chen and D. L. Jones, "A Real-Time 3D Sound Localization System with Miniature Microphone Array for Virtual Reality," *Proceedings of IEEE Conference on Industrial Electronics and Applications*, July 2012.

[56] L. Wan and D. Chen, "CCP: Common Case Promotion for Improved Timing Error Resilience with Energy Efficiency," *Proceedings of IEEE/ACM International Symposium on Low Power Electronics and Design*, July 2012.

[57] H. Luo, S. Wei, D. Chen, and D. Guo, "Hybrid Circuit-Switched NOC for Low Cost On-chip Communication", *Proceedings of IEEE International Conference on Anti-Counterfeiting, Security and Identification*, August, 2012.

[58] Z. Zhang and D. Chen, "Challenges and Opportunities of ESL Design Automation", *Proceedings of IEEE International Conference on Solid-State and Integrated Circuit Technology*, October 2012. (**Invited**)

[59] S. Gurumani, K. Rupnow, Y. Liang, H. Cholakkail, and D. Chen, "High Level Synthesis of Multiple Dependent CUDA Kernels for FPGAs," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2013. (**Invited**)

[60] Y. Liang, Z. Cui, K. Rupnow, and D. Chen, "Register and Thread Structure Optimization for GPUs," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2013.

[61] W. Zuo, Y. Liang, K. Rupnow, P. Li, D. Chen, and J. Cong, "Improving High Level Synthesis Optimization Opportunity Through Polyhedral Transformations," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2013.

[62] Y. Liang, H. P. Huynh, K. Rupnow, R. Goh, and D. Chen, "Efficient Concurrent Kernel Execution on GPUs", *Proceedings of Workshop on SoCs, Heterogeneous Architectures and Workloads*, February, 2013.

[63] Y-Y. Chen, A. Rogachev, A. Sangai, G. Iannaccone, G. Fiori, and D. Chen, "A SPICE-Compatible Model of Graphene Nano-Ribbon Field-Effect Transistors Enabling Circuit-Level Delay and Power Analysis Under Process Variation," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2013.

[64] A. Papakonstantinou, D. Chen, W.M. Hwu, J. Cong, and Y. Liang, "Throughput-oriented Kernel Porting onto FPGAs," *Proceedings of IEEE/ACM Design Automation Conference*, June 2013.

[65] Y-Y. Chen, A. Sangai, M. Gholipour, and D. Chen, "Schottky-Barrier-Type Graphene Nano-Ribbon Field-Effect Transistors: A Study on Compact Modeling, Process Variation, and Circuit Performance," *Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures*, July 2013.

[66] H. Zheng, S. Gurumani, L. Yang, D. Chen, K. Rupnow, "High-level Synthesis with Behavioral level Multi-Cycle Path Analysis," *Proceedings of IEEE International Conference on Field Programmable Logic and Applications*, September, 2013.

[67] Y-Y. Chen, A. Sangai, M. Gholipour, and D. Chen, "Graphene Nano-Ribbon Field-Effect Transistors as Future Low-Power Devices," *Proceedings of IEEE/ACM International Symposium on Low Power Electronics and Design*, September 2013. **(Invited)**

[68] W. Zuo, P. Li, D. Chen, L-N. Pouchet, S. Zhong, and J. Cong, "Improving Polyhedral Code Generation for High-Level Synthesis," *Proceedings of IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis*, September 2013. (**Best Paper Award**)

[69] X. Xie, Y. Liang, G. Sun, and D. Chen, "An Efficient Compiler Framework for Cache Bypassing on GPUs," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2013.

[70] S. T. C. Konigsmark, L. Hwang, D. Chen, and D. F. Wong, "CNPUF: A Carbon Nanotube-based Physically Unclonable Function for Secure Low-Energy Hardware Design," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2014.

[71] Y. Liang and D. Chen, "Fast Large-Scale Optimal Power Flow Analysis for Smart Grid through Network Reduction," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2014.

[72] H. Zheng, S. Gurumani, K. Rupnow, and D. Chen, "Fast and Effective Placement and Routing Directed High-Level Synthesis for FPGAs," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2014.

[73] M. Gholipour, Y-Y Chen, A. Sangai, and D. Chen, "Highly Accurate SPICE-Compatible Modeling for Single- and Double-Gate GNRFETs with Studies on Technology Scaling," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2014.

[74] S. Gurumani, J. Tolar, Y. Chen, Y. Liang, K. Rupnow, and D. Chen, "Integrated CUDA-to-FPGA Synthesis with Network-on-Chip," *Proceedings of IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2014.

[75] C.H. Lin, L. Wan, and D. Chen, "C-Mine: Data Mining of Logic Common Cases for Low Power Synthesis of Better-Than-Worst-Case Designs," *Proceedings of IEEE/ACM Design Automation Conference*, June 2014.

[76] Y. Liang and D. Chen, "ClusRed: Clustering and Network Reduction-based Probabilistic Optimal Power Flow Analysis for Large-scale Smart Grids," *Proceedings of IEEE/ACM Design Automation Conference*, June 2014.

[77] R. Mancuso, P. Srivastava, D. Chen, and M. Caccamo, "A Hardware Architecture to Deploy Complex Multiprocessor Scheduling Algorithms," *Proceedings of IEEE International Conference on Embedded and Real-Time Computing Systems and Applications*, August 2014.

[78] J. Wang, A. Dhar, D. Chen, Y. Liang, Y. Wang, and B. Guo "Workload Allocation and Thread Structure Optimization for MapReduce on GPUs," *Proceedings of SRC Technical Conference (TECHCON)*, September 2014.

[79] Y. Liang and D. Chen, "New Algorithms for Computation Acceleration for Large-scale Smart Grids," *Proceedings of IEEE International Conference on Solid-State and Integrated Circuit Technology*, October 2014. (**Invited**)

[80] S. T. C. Konigsmark, L. Hwang, D. F. Wong, and D. Chen, "System-of-PUFs: Multilevel Security for Embedded Systems," *Proceedings of IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis*, October 2014.

[81] W. Zuo, H. Zheng, S. Gurumani, K. Rupnow, and D. Chen, "New Solutions for System-Level and High-Level Synthesis," *Proceedings of IEEE International Symposium on Integrated Circuits*, December 2014. (**Invited**)

[82] C. Wei, A. Dhar, and D. Chen, "A Scalable and High-Density FPGA Architecture with Multi-Level Phase Change Memory," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2015.

[83] A. Ramachandran, Y. Heo, W.M. Hwu, J. Ma, and D. Chen, "FPGA Accelerated DNA Error Correction," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2015.

[84] K. Campbell, D. Lin, S. Mitra, and D. Chen, "Hybrid Quick Error Detection (H-QED): Accelerator Validation and Debug using High-Level Synthesis Principles," *Proceedings of IEEE/ACM Design Automation Conference*, June 2015.

[85] K. Campbell, P. Vissa, D. Z. Pan, and D. Chen, "High-Level Synthesis of Error Detecting Cores through Low-Cost Modulo-3 Shadow Datapaths," *Proceedings of IEEE/ACM Design Automation Conference*, June 2015.

[86] Y.Y. Chen, Z. Sun, and D. Chen "A SPICE Model for Flexible Transition Metal Dichalcogenide Field-Effect Transistors," *Proceedings of IEEE/ACM Design Automation Conference*, June 2015.

[87] C. Zhuge, C.W. Lung, D. Chen, and Y.K. Jan, "Development of the Feedback Controlled Indentation System for Assessing Risk of Pressure Ulcers," *Proceedings of Rehabilitation Engineering and Assistive Technology Society of North America (RESNA) Annual Conference*, June 2015.

[88] Y. Liang, H. Zhu, and D. Chen, "Optimal Blocker Placement for Mitigating the Effects of Geomagnetic Induced Currents Using Branch and Cut Algorithm," *Proceedings of North American Power Symposium (NAPS)*, October 2015

[89] C. H. Lin, S. Roy, C. Y. Wang, D. Z. Pan, and D. Chen, "CSL: Coordinated and Scalable Logic Synthesis Techniques for Effective NBTI Reduction," *Proceedings of IEEE International Conference on Computer Design*, October 2015.

[90] W. Zuo, W. Kemmerer, J. B. Lim, L.-N. Pochet, A. Ayupoy, T. Kim, K. Han, and D. Chen, "A polyhedral-based SystemC modeling and generation framework for effective low-power design space exploration," *Proceedings of IEEE/ACM International Conference* on *Computer-Aided Design*, November 2015. (**Best Paper Award**)

[91] M. Potkonjak, D. Chen, P. Kalla, and S. P. Levitan, "DA Vision 2015: From Here to Eternity," *Proceedings of IEEE/ACM International Conference* on *Computer-Aided Design*, November 2015. (**Invited**)

[92] L. Yang, Y. Chen, W. Zuo, T. Nguyen, S. Gurumani, K. Rupnow, and D. Chen, "System-Level Design Solutions: Enabling the IoT Explosion," *Proceedings of IEEE International Conference on ASIC*, November 2015. (**Invited**)

[93] L. Yang, S. Gurumani, D. Chen, and K. Rupnow, "Behavioral-Level IP Integration in High-Level Synthesis," *Proceedings of International Conference on Field-Programmable Technology*, December 2015.

[94] L. Yang, M. Ikram, S. Gurumani, D. Chen, S. Fahmy, and K. Rupnow, "JIT Trace-based Verification for High-Level Synthesis," *Proceedings of International Conference on Field-Programmable Technology*, December 2015.

[95] Z. Sun, K. Campbell, W. Zuo, K. Rupnow, S. Gurumani, F. Doucet, and D. Chen, "Designing High-Quality Hardware on a Development Effort Budget: A Study of the Current State of High-Level

Synthesis", *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2016. (**Invited**)

[96] Y-Y Chen, M. Gholipour, and D. Chen, "Flexible Transition Metal Dichalcogenide Field-Effect Transistors: A Circuit-Level Simulation Study of Delay and Power under Bending, Process Variation, and Scaling," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2016.

[97] T. Nguyen, S. Gurumani, K. Rupnow, and D. Chen, "FCUDA-SoC: Platform Integration for Field-Programmable SoC with the CUDA-to-FPGA Compiler," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2016.

[98] X. Liu, Y. Chen, T. Nguyen, S. Gurumani, K. Rupnow, and D. Chen, "High Level Synthesis of Complex Applications: An H.264 Video Decoder", *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2016.

[99] M. T. Satria, W. Zheng, S. Gurumani, K. P. Tee, A. Koh, P. Yu, K. Rupnow, and D. Chen, "Real-Time System-Level Implementation of a Telepresence Robot Using an Embedded GPU Platform," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2016.

[100] L. Yang, S. Gurumani, D. Chen, and K. Rupnow, "AutoSLIDE: Automatic Source-Level Instrumentation and Debugging for HLS," *Proceedings of IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016.

[101] K. Campbell, L. He, L. Yang, S. Gurumani, K. Rupnow, and D. Chen, "Debugging and Verifying SoC Designs through Effective Cross-Layer Hardware-Software Co-simulation," *Proceedings of IEEE/ACM Design Automation Conference*, June 2016.

[102] S. T. C. Konigsmark, D. F. Wong, and D. Chen, "Information Dispersion for Trojan Defense through High-Level Synthesis," *Proceedings of IEEE/ACM Design Automation Conference*, June 2016.

[103] T. Nguyen, Y. Chen, K. Rupnow, S. Gurumani, and D. Chen, "SoC, NoC and Hierarchical Bus Implementations of Applications on FPGAs Using the FCUDA Flow", *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, July 2016. **(Invited)**

[104] W. Kemmerer, W. Zuo, and D. Chen, "Parallel Code-Specific CPU Simulation with Dynamic Phase Convergence Modeling for HW/SW Co-Design", *Proceedings of IEEE/ACM International Conference* on *Computer-Aided Design*, November 2016.

[105] S. Huang, G. J. Manikandan, A. Ramachandran, K. Rupnow, W.M. Hwu, and D. Chen, "Hardware Acceleration of the Pair-HMM Algorithm for DNA Variant Calling", *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2017.

[106] L.W. Chang, J. Gómez-Luna, I. Hajj, S. Huang, D. Chen, and W.M. Hwu, "Collaborative Computing for Heterogeneous Integrated Systems," *Proceedings of ACM/SPEC International Conference on Performance Engineering*, April 2017.

[107] A. Dhar and D. Chen, "Efficient GPGPU Computing with Cross-Core Resource Sharing and Core Reconfiguration," *Proceedings of IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2017.

[108] W. Zuo, T. Kim, A. Ayupov, C.W Lin, S. Shiraishi, L.N. Pouchet, and D. Chen, "Accurate High-level Modeling and Automated Hardware/Software Co-design for Effective SoC Design Space Exploration," *Proceedings of IEEE/ACM Design Automation Conference*, June 2017.

[109] Sven Tenzing Choden Konigsmark, Deming Chen, and Martin Wong, "High-Level Synthesis for Side-Channel Defense," *Proceedings of IEEE International Conference on Application-specific*

Systems, Architectures and Processors, July 2017.

[110] Di He, Zuofu Cheng, Mark Hasegawa-Johnson, and Deming Chen, "Using Approximated Auditory Roughness as a Pre-filtering Feature for Human Screaming and Affective Speech AED," *Proceedings of Annual Conference of the International Speech Communication Association*, August 2017.

[111] Xiaofan Zhang, Xinheng Liu, Anand Ramachandran, Chuanhao Zhuge, Shibin Tang, Peng ouyang, Zuofu Cheng, Kyle Rupnow and Deming Chen, "High-Performance Video Content Recognition with Long-term Recurrent Convolutional Network for FPGA", *Proceedings of International Conference on Field-Programmable Logic and Applications*, September 2017.

[112] Sitao Huang, Simon Garcia De Gonzalo, Li-Wen Chang, Izzat El Hajj, Juan Gómez-Luna, Sai Rahul Chalamalasetti, Mohamed El Hadedy, Dejan Milojicic, Deming Chen, and Wen-mei Hwu, "Collaborative Computing on Heterogeneous CPU-FPGA Systems", *Proceedings of TECHCON*, September 2017.

[113] Keith Campbell, Eric Cheng, Subhasish Mitra, and Deming Chen, "Cost-Effective Cross-Layer Resilience for Hardware Accelerators," *Proceedings of TECHCON*, September 2017.

[114] Wen-mei Hwu, Izzat El Hajj, Simon Garcia de Gonzalo, Carl Pearson, Nam Sung Kim, Deming Chen, Jinjun Xiong, and Zehra Sura, "Rebooting the Data Access Hierarchy of Computing Systems," *Proceedings of IEEE International Conference on Rebooting Computing (ICRC)*, November 2017. (**Invited**)

[115] Xiaofan Zhang, Anand Ramachandran, Chuanhao Zhuge, Di He, Wei Zuo, Zuofu Cheng, Kyle Rupnow, and Deming Chen, "Machine Learning on FPGAs to Face the IoT Revolution," *Proceedings of IEEE/ACM International Conference* on *Computer-Aided Design*, November 2017. (**Invited**)

[116] Eric Cheng, Jacob Abraham, Pradip Bose, Alper Buyuktosunoglu, Keith Campbell, Deming Chen, Cheng-Yong Cher, Hyungmin Cho, Binh Le, Klas Lilja, Shahrzad Mirkhani, Kevin Skadron, Mircea Stan, Lukasz Szafaryn8, Christos Vezyrtzis, and Subhasish Mitra, "Cross-Layer Resilience in Low-Voltage Digital Systems: Key Insights," *Proceedings of IEEE International Conference on Computer Design*, November 2017. **(Invited)**

[117] Keith Campbell, Chen-Hsuan Lin, and Deming Chen, "Low-Cost Hardware Architectures for Mersenne Modulo Functional Units", *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2018.

[118] Anand Ramachandran, Huiren Li, Eric Klee, Steven Lumetta, and Deming Chen, "Deep Learning for Better Variant Calling for Cancer Diagnosis and Treatment", *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2018. **(Invited)**

[119] Chuanhao Zhuge, Xinheng Liu, Xiaofan Zhang, Sudeep Gummadi, Jinjun Xiong, and Deming Chen, "Face Recognition with Hybrid Efficient Convolution Algorithms on FPGAs," *Proceedings of ACM/IEEE Great Lakes Symposium on VLSI*, May 2018.

[120] Y. Li, X. Zhang and D. Chen, "CSRNet: Dilated Convolutional Neural Networks for Understanding the Highly Congested Scenes," *Proceedings of Conference on Computer Vision and Pattern Recognition*, June 2018.

[121] Xinheng Liu, Dae Hee Kim, Chang Wu and Deming Chen, "Resource and Data Optimization for Hardware Implementation of Deep Neural Networks Targeting FPGA-based Edge Devices", *Proceedings of IEEE/ACM International Workshop on System-Level Interconnect Prediction*, June 2018. **(Best Paper Award)**

[122] Huiren Li, Anand Ramachandran, and Deming Chen, "GPU Acceleration of Advanced *k*-mer Counting for Computational Genomics", *Proceedings of IEEE International Conference on*

Application-specific Systems, Architectures and Processors, July 2018.

[123] Junsong Wang, Qiuwen Lou, Xiaofan Zhang, Chao Zhu, Yonghua Lin and Deming Chen, "A Design Flow of Accelerating Hybrid Extremely Low Bit-width Neural Network in Embedded FPGA", *Proceedings of International Conference on Field-Programmable Logic and Applications*, August 2018.

[124] Di He, Boon Pang Lim, Xuesong Yang, Mark Hasegawa-Johnson, and Deming Chen, "Improved ASR for Under-Resourced Languages Through Multi-Task Learning with Acoustic Landmarks", *Proceedings of Annual Conference of the International Speech Communication Association*, September 2018.

[125] Sitao Huang, Mohamed El-Hadedy, Cong Hao, Qin Li, Vikram Sharma Mailthody, Ketan Date, Jinjun Xiong, Deming Chen, Rakesh Nagi and Wen-Mei Hwu, "Triangle Counting and Truss Decomposition using FPGA," *Proceedings of IEEE High Performance Extreme Computing Conference (HPEC)*, September 2018. **(Student Innovation Award)**

[126] Mohammad Alian, Seung Won Min, Hadi Asgharimoghaddam, Ashutosh Dhar, Dong Kai Wang, Thomas Roewer, Adam McPadden, Oliver OHalloran, Deming Chen, Jinjun Xiong, Daehoon Kim, Wen-mei Hwu, and Nam Sung Kim, "Application-transparent near-memory processing architecture with memory channel network," *Proceedings of IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October, 2018. **(Best Paper Award Candidate)**

[127] Cong Hao and Deming Chen, "Deep Neural Network Model and FPGA Accelerator Co-design: Opportunities and Challenges", *Proceedings of IEEE International Conference on Solid-State and Integrated Circuit Technology*, October 2018. **(Invited)**

[128] Xiaofan Zhang, Junsong Wang, Chao Zhu, Yonghua Lin, Jinjun Xiong, Wen-mei Hwu, and Deming Chen, "DNNBuilder: an Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs", *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2018. **(Best Paper Award)**

[129] Qin Li, Xiaofan Zhang, Jinjun Xiong, Wen-mei Hwu, and Deming Chen, "Implementing Neural Machine Translation with Bi-Directional GRU and Attention Mechanism on FPGAs Using HLS," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2019.

[130] Yao Chen, Jiong He, Xiaofan Zhang, Cong Hao, and Deming Chen, "Cloud-DNN: An Open Framework for Mapping DNN Models to Cloud FPGAs", *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2019.

[131] Sitao Huang, Li-Wen Chang, Izzat El Hajj, Simon Garcia de Gonzalo, Juan Gómez Luna, Sai Rahul Chalamalasetti, Mohamed El-Hadedy, Dejan Milojicic, Onur Mutlu, Deming Chen, and Wen-mei Hwu, "Collaborative Computing on Heterogeneous CPU-FPGA Architectures Using OpenCL," *Proceedings of ACM/SPEC International Conference on Performance Engineering*, Apr. 2019.

[132] Anand Ramachandran, Eric Klee, Steven Lumetta, and Deming Chen, "A Recurrent Markov State-space Generative Model for Sequences," *Proceedings of International Conference on Artificial Intelligence and Statistics*, Apr. 2019.

Other Workshop Papers, Poster Papers, Journal Abstract, or Online Publications

[1] C. Dong, S. Chilstedt, and D. Chen, "Variation Aware Routing for Three-Dimensional FPGAs," *Workshop on 3D Integration and Interconnect-Centric Architectures*, Feb. 2009. (A later version with the same title appeared in *IEEE Computer Society Annual Symposium on VLSI*, May 2009.)

[2] A. Papakonstantinou, K. Gururaj, J. Stratton, D. Chen, J. Cong, and W.M. Hwu, "High-Performance CUDA Kernel Execution on FPGAs," *International Conference on Supercomputing*, June 2009. (Two-page extended abstract in the proceeding.)

[3] D. Chen, S. Chilstedt, C. Dong, and E. Pop, "What Everyone Needs to Know about Carbon-Based Nanocircuits," *Online Knowledge Center, Topic: Back-End, Sub-topic: New Technologies and Directions, IEEE/ACM Design Automation Conference*, 2010. (**Invited**)

[4] L. Wan and D. Chen, "Circuit Level Dynamic Behavior Analysis through Timed Ternary Decision Diagram," *Proceedings of IEEE/ACM International Workshop on Logic & Synthesis*, June 2010.

[5] K. Rupnow, Y. Liang, D. Min, M. Do and D. Chen, "Mobile 3D Vision - Algorithm and Platform Challenges," *FPL Workshop on Computer Vision on Low-Power Reconfigurable Architectures*, 2011.

[6] Y-Y. Chen, A. Rogachev, A. Sangai, G. Iannaccone, G. Fiori, and D. Chen, "A SPICE-compatible Model of Graphene Nano-Ribbon Field-Effect Transistors", *NSF Workshop on Nano and Micro Manufacturing*, May 2013.

[7] Y-Y Chen, A. Sangai, M. Gholipour, and D. Chen, "Effects of Process Variation on the Circuit-Level Performance of Graphene Nano-Ribbon Field-Effect Transistors," *Workshop on Variability Modeling and Characterization*, Nov. 2013.

[8] A. Dhar and D. Chen, "Neuromorphic Architecture Inspired Fast, Efficient and Configurable On-Chip Learning Via In-Memory Computing and RRAM", Poster paper, *2015 Workshop on Hardware and Algorithms for Learning On-a-chip (HALO)*, Nov. 2015.

[9] D. Chen, J. Cong, S. Gurumani, W.M. Hwu, K. Rupnow, and Z. Zhang, "System Synthesis and Automated Verification: Design Demands for IoT Devices," *Sensors to Cloud Architectures Workshop*, March 2016.

[10] Di He, Boon Pang Lim, Xuesong Yang, Mark Hasegawa-Johnson, and Deming Chen, "Selecting frames for automatic speech recognition based on acoustic landmarks," *The Journal of the Acoustical Society of America*, 141(5):3468-3468, May 2017. DOI: 10.1121/1.4987204.

[11] Xiaofan Zhang, Mohamed El Hadedy, Wen-mei Hwu, Nam Sung Kim, Jinjun Xiong, and Deming Chen, "Implementing Long-term Recurrent Convolutional Network Using HLS on POWER System," *IBM OpenPOWER Summit*, Las Vegas, 2018.

[12] Junsong Wang, Qiuwen Lou, Xiaofan Zhang, Chao Zhu, Yonghua Lin, and Deming Chen, "A Design Flow of Accelerating Hybrid Extremely Low Bit-width Neural Network in Embedded FPGA," *Design Automation Conference (DAC) Late Breaking Results*, San Francisco, 2018.

Ph.D. Thesis

- *Design and Synthesis for Low-Power FPGAs*, Computer Science Department, University of California at Los Angeles, 2005. (Ph.D. advisor: Prof. Jason Cong).

Tool Releases

- **GNRFET HSPICE Model**: First parameterized HSPICE transistor compact models of two types of Graphene Nano-Ribbon Field-Effect Transistors, MOS-GNRFET and SB-GNRFET. Available at nanoHUB.org since July 2013. (about 2000 downloads so far.)

  Download: http://dchen.ece.illinois.edu/tools.html

- **BLESS**: Bloom-filter-based Error Correction Solution for High throughput Sequencing Reads. Currently, the best DNA error correction tool in terms of quality and small memory usage. Available since January 2014. (about 3000 downloads so far.)

  Download: http://dchen.ece.illinois.edu/tools.html

- **TIGER**: Tiled Iterative Genome Assembler. Significant improvement over state-of-the-art *de novo* genome assemblers. Available since 2013.

  Download: http://impact.crhc.illinois.edu/Tiger/tiger.aspx

- **H.264 HLS Benchmark**: Fully synthesizable H.264 Video Decoder code, which can be synthesized into RTL with high-level synthesis for FPGA implementation and achieve real-time decoding.

  Download: http://dchen.ece.illinois.edu/tools.html

- **TMDFET SPICE Model**: SPICE transistor models of flexible Transition Metal Dichalcogenide Field-Effect Transistors, TMDFET.

  Download: http://dchen.ece.illinois.edu/tools.html

- **FCUDA**: **Open Source.** A system-synthesis compiler to map GPU CUDA code to FPGA. Enable a common frontend language for heterogeneous compute platforms where FPGA and GPU co-exist. Low-power FPGA computing with comparable performance as GPU.

  Download: http://dchen.ece.illinois.edu/tools.html

- **NEW! RIP**: **Open Source.** This open source project contains three inter-related software packages (fast software modeling, fast hardware modeling and design space exploration, and hardware/software co-design), for the ultimate task of automated hardware/software partitioning targeting either sophisticated SoC designs or computing on heterogeneous systems.

  Download: https://github.com/UIUC-ChenLab/rip

Patents and Licenses

- Patent filed from UIUC/Stanford, 2016.
  Title: "Fast and High-Coverage Post-Silicon Validation for Complex SoCs with Accelerators."
  Co-inventors: Keith A. Campbell, Hai Lin, Deming Chen, Subhasish Mitra.
- Technology license: AutoESL Inc. licensed the xPilot technology out of UCLA, 2006.
  Co-inventors: Deming Chen, Jason Cong, Yiping Fan, Guoling Han, Wei Jiang, and Zhiru Zhang.
  Title: "xPilot: A Platform-Based Behavioral Synthesis System".
  This technology eventually led to the acquisition of AutoESL by Xilinx. xPilot became the high-level synthesis engine of Xilinx Vivado HLS (high-level synthesis).
- Technology license: Inspirit IoT, Inc. licensed the VAST HLS technology out of ADSC/UIUC, 2016.
  Co-inventors: Deming Chen, Hongbin Zheng, Kyle Rupnow, Swathi Gurumani.
  Title: "VAST: High-level Synthesis Tool".
- Technology license: a company licensed the RASP technology out of UCLA, 2017.
  Co-inventors: Deming Chen, Jason Cong, Eugene Ding, Zhijun Huang, Yeanyow Hwang, Chang Wu, Sarah Xu.
  Title: "RASP: FPGA/CPLD Technology Mapping and Synthesis Package".

University Services

- Elected into the Senate of University of Illinois, 2018-2019
- Invited reviewer for proposals for CoE's SRI Program, 2018
- Elected into the Executive Committee of College of Engineering, 2016-2019
- ECE Promotion and Tenure Committee, 2016-2019
- Area Chair, Computer Engineering, 2015-2017
- Elected into the Senate of University of Illinois, 2013-2016
- Panelist, campus review panel for GYSS travel grant competition, 2015
- Alternate representative of CSL on the College Executive Committee, 2015-2016
- CSL Director Search Committee, 2014
- Chair, CE Lecturer Search Committee, 2014
- Member, EE Lecturer Search Committee, 2014
- ECE Curriculum Committee, 2013-2014
- CSL Policy and Planning Committee, 2008-2009, 2011-2012, 2014-2016
- Computer Engineering Committee, 2008-2015
- Member of Teaching Evaluation and Awards Committee, 2005-2007
- Graduate ECE Seminar Committee, 2006-2007, 2009
- Graduate Committee, 2007-2009, 2011-2012
- Fellowship Committee, 2009-2012
- Colloquium Committee, 2010-2014
- CSL Build-out Committee, 2012
- Ph.D. committees:
  - 2006: Dr. Smruti Sarangi (CS, UIUC), Dr. Lei Cheng (CS, UIUC)
  - 2007: Dr. Liang Deng (ECE, UIUC), Dr. Yu Zhong (ECE, UIUC), Mr. Sain-Zee Ueng (ECE, UIUC), Dr. Yidnek Mekonnen (ECE, UIUC), Dr. Radu Teodorescu (CS, UIUC)
  - 2008: Dr. Zhiguo Qian (ECE, UIUC), Dr. Tomasz Czajkowski (ECE, U. of Toronto), Dr. Brian Greskamp (CS, UIUC), Dr. Rodolfo Pellizoni (CS, UIUC)
  - 2009: Dr. Chen Dong (ECE, UIUC)
  - 2010: Dr. Hui Kong (ECE, UIUC), Dr. Tan Yan (ECE, UIUC), Dr. John Kelm (ECE, UIUC), Dr. Lijuan Luo (ECE, UIUC), Dr. Lu Wan (ECE, UIUC), Dr. Yingying Kuai (ECE, UIUC)
  - 2011: Dr. Alex Papakonstantinou (ECE, UIUC), Dr. Joon Hyung Chung (ECE, UIUC), Dr. Neal Crago (ECE, UIUC), Dr. Hongbo Zhang (ECE, UIUC)
  - 2012: Dr. Qiang Ma (ECE, UIUC), Dr. John Stratton (ECE, UIUC), Dr. Xiao-Long Wu (ECE, UIUC), Dr. Feng Xiong (ECE, UIUC)
  - 2013: Dr. Yuelin Du (ECE, UIUC), Dr. Ting Yu (ECE, UIUC), Dr. Soobae Kim (ECE, UIUC)
  - 2014: Dr. Eric Kim (ECE, UIUC),
  - 2015: Dr. Rajesh Bhana (ECE, UIUC), Dr. Yun Heo (ECE, UIUC), Dr. Hee-Seok Kim (ECE, UIUC), Dr. Christine Ying-Yu Chen (ECE, UIUC), Dr. Jungwook Choi (ECE, UIUC), Dr. Pei-Ci Wu (ECE, UIUC), Dr. Kuo-Hsuan Meng (ECE, UIUC), Dr. Joe Meng (ECE, UIUC).
  - 2016: Mr. Yi Liang (ECE, UIUC), Dr. Maryam Kazerooni (ECE, UIUC), Dr. Haitong Tian (ECE, UIUC), Dr. Jongsok Choi (External Examiner, ECE, U. of Toronto).
  - 2017: Dr. Choden Konigsmark (ECE, UIUC), Dr. Siming Guo (ECE, UIUC), Dr. Wonhyeok Jang (ECE, UIUC), Dr. Tsung-Wei Huang (ECE, UIUC), Dr. Henry Duwe (ECE, UIUC), Dr. Romesh Nandwana (ECE, UIUC), Dr. Nicholas Thomson (ECE, UIUC), Dr. Keith Campbell (ECE, UIUC), Dr. Glenn Ko (CS, UIUC), Dr. Chen-Hsuan Lin (ECE, UIUC), Dr. Ti Xu (ECE, UIUC), Mr. Daifeng Guo (ECE, UIUC), Mr. Di He (ECE, UIUC), Ms. Wei Zuo (ECE, UIUC), Dr. Guanwen Zhong (External Examiner, CS, National U of

Singapore), Dr. Hao Liang (External Examiner, ECE, Hong Kong U of Science and Technology).

2018: Dr. Johnathan Alsop (ECE, UIUC), Dr. Izzat El Hajj (ECE, UIUC), Dr. Leslie Hwang (ECE, UIUC), Mr. Tianqi Gao (ECE, UIUC), Mr. Chun Xun Lin (ECE, UIUC).

Invited Talks

Title	Conference or Seminar	Location	Year
Design and Synthesis for Low-Power FPGAs	Seminar	Altera Corp., San Jose	2005
VLSI design: turning your big ideas into reality	ECE 200: Undergraduate Seminar	UIUC	2006
Technology Mapping Algorithms for Programmable Logic Devices	ECE 500: Graduate Seminar	UIUC	2006
Abstraction beyond RTL for Low-Power	Computer Engineering Seminar	UIUC	2006
Design and Synthesis for Low-Power FPGAs	Seminar	Velogix Inc., San Jose	2006
3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA Architecture	ECE 590B: Electromagnetics, Optics & Remote Sensing Seminar	UIUC	2007
System, Behavioral, and Logic Level Design Automation	Seminar	T.J. Watson Research Center, IBM, USA	2007
3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA Architecture	Computer Engineering/Circuits Seminar	UIUC	2007
3D nFPGA: A CMOS/Nanomaterial Hybrid Reconfigurable Architecture	Workshop on SoC Design Methodologies	Seoul National University, Seoul, Korea	2007
Design and Synthesis for Low-Power FPGAs	Seminar	Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China	2007
VEBoC: Variation and Error-Aware Design for Billions of Devices on a Chip	IEEE/ACM Asia and South Pacific Design Automation Conference	Seoul, Korea	2008
New Design Techniques and Architectures for FPGAs	ECE Seminar	University of Toronto, Toronto, Canada	2008
New Design Techniques and Architectures for FPGAs	Seminar	Altera Corp., Toronto	2008
New Design Techniques and Architectures for FPGAs	Seminar	Xilinx Corp., Toronto	2008
EPOS: an Explicitly Parallel Operations System	Workshop of SoC Design Methodologies	National Tsing Hua University, Taiwan	2008
New Synthesis and Architecture Solutions for Reconfigurable ICs	DLP and VLSI/CAD Workshop	National Tsing Hua University, Taiwan	2008
New Synthesis and Architecture Solutions for Reconfigurable ICs	EE Seminar	National Taiwan University, Taiwan	2008
Variation-Aware Chip Design for Reliability and Performance	Seminar	Sun Microsystems, Inc., USA	2008
Reconfigurable Circuits Design with Nanomaterials	Design, Automation and Test in Europe (DATE)	Nice, France	2009
New Binding Algorithms for Glitch	ECSI and USB Workshop on	Yokohama, Japan	2009

and Inter-transition Power Reduction	High Level Synthesis: Next Step to Efficient ESL Design		
Nano 3D FPGAs: Design and CAD	Seminar	T.J. Watson Research Center, IBM, USA	2009
FPCNA: A Field Programmable Carbon Nanotube Array	Global COE Workshop	Wasada University, Japan	2009
Design and CAD for Nanoscale Reconfigurable Logic	EE Seminar	Stanford University	2009
New Design Techniques for Existing and Futuristic FPGAs	EECS Seminar	UC Berkeley	2009
Reconfigurable Computing for High Performance	CS Seminar	National University of Singapore	2010
Reconfigurable Computing for High Performance	CE Seminar	Nanyang Technological University, Singapore	2010
New Design Techniques for Existing and Futuristic FPGAs	CSSI Seminar	Carnegie Mellon University	2010
Challenges and Opportunities of ESL Design Automation	Electronic Design Processes Symposium	Monterey, CA	2010
Compilation and Optimization for High Performance	ECE Seminar	Purdue University	2010
FCUDA: Enabling Efficient Compilation of CUDA Kernels onto FPGAs	Asia South Pacific Design Automation Workshop	Incheon, Korea	2010
Challenges and Opportunities of ESL Design Automation	Electronic Design Processes Symposium	Monterey, CA	2010
FCUDA: Efficient CUDA Kernel Compilation for High-Performance Computing on FPGAs	Seminar	NEC, Tokyo, Japan	2011
3D FPGAs with Nanotechnology	NYU-AD 3D Workshop	Abu Dhabi, United Arab Emirates	2011
Porting Performance across GPUs and FPGAs	Pre-conference Workshop at FCCM	Salt Lake City, Utah	2011
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	eSeminar	GSRC (Gigascale Systems Research Center), USA	2011
Design and CAD for 3D Reconfigurable Circuits	Symposium on 3D TSV Processes and Design Challenges	Singapore	2011
FCUDA: Porting Performance across GPUs and FPGAs	Web seminar	Intel, Oregon	2011
High Level Synthesis of FPGA and Future Nanoscale FPGA Design	Graduate Seminar, School of Information Science and Technology, Xiamen University	Xiamen, China	2011
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	PIC Seminar, IBM	T.J. Watson Research Center, Yorktown Heights	2011
3D FPGAs with Nanotechnology	Nanoelectronic Devices for Defense & Security Conference	New York	2011

High-level Synthesis for FPGA and Futuristic 3D FPGA Design	Departmental Seminar	National Taiwan University	2011
High-level Synthesis for FPGA and Futuristic 3D FPGA Design	Departmental Seminar	National Tsing Hua University, Taiwan	2011
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	Departmental Seminar	University of Wisconsin at Madison	2012
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	Departmental Seminar	University of Illinois at Chicago	2012
Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	AMD Research Center, Beijing	2012
Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	Tsinghua University, China	2012
Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	Microsoft Research Center, Beijing	2012
Control Flow Optimization for GPU Computing and Other Research Highlights	Special CS Seminar	Stanford University	2012
GPU Computing and the CUDA-to-FPGA Compiler	Departmental Seminar	University of California at Riverside	2012
GPU Computing and the CUDA-to-FPGA Compiler	Invited panel presentation	T.J. Watson Research Center, Yorktown Heights	2013
GPU Computing and the CUDA-to-FPGA Compiler	Departmental Seminar	Imperial College, London	2013
Optimizations in GPU: Smart Compilers and Core-level Reconfiguration	ACM/IEEE System Level Interconnect Prediction	Austin, TX	2013
Is Graphene Useful for Digital Circuits?	EDA Workshop	Kyoto, Japan	2013
Graphene Nano-Ribbon Field-Effect Transistors as Future Low-Power Devices	IEEE/ACM International Symposium on Low Power Electronics and Design	Beijing, China	2013
Compiler Optimization for GPU Computing	Departmental Seminar	National Taiwan University, Taiwan	2014
Compiler Optimization for GPU Computing	Special Seminar	National Chiao Tung University, Taiwan	2014
New Solutions for High-level Synthesis	Special Seminar	University of Southern California	2014
New Solutions for System and High-level Synthesis	Special Seminar	Harvard University	2014

New Solutions for High Level Synthesis	eSeminar	C-FAR Research Center	2014
New Solutions for System and High-level Synthesis	CS Seminar	School of Computing, National University of Singapore	2014
New Algorithms for Computation Acceleration for Large-scale Smart Grids	IEEE International Conference on Solid-State and Integrated Circuit Technology	Guilin, China	2014
FCUDA: the CUDA to FPGA Compiler	ICCAD 2014 Workshop: Heterogeneous Computing Platforms (HCP)	San Jose, CA	2014
New Solutions for System-Level and High-Level Synthesis	IEEE International Symposium on Integrated Circuits	Singapore	2014
Reliability, Security, and Design Productivity in the Era of IoT	IEEE International Conference on Anti-counterfeiting, Security, and Identification	Macau, China	2014
Boosting Design Productivity for the Internet of Billons of Things	Advanced Digital Sciences Center	Singapore	2014
Quantifying and Improving the Accuracy of Detecting Genomic Variation	NSF I/UCRC Planning Workshop	Chicago, IL	2015
Boosting Design Productivity for the Internet of Billons of Things	China Semiconductor Technology International Conference (CSTIC)	Shanghai, China	2015
Improving Design Productivity for High-Performance and Energy-Efficient Circuits	Special Seminar	Qualcomm, San Jose	2015
New High-level Synthesis Techniques for High-Performance, Energy-Efficiency, and Reliability	Special Seminar	University of Bologna, Bologna, Italy	2015
High Design Productivity for Reliable and Energy-Efficient Circuits in the Era of Internet of Things	Special Seminar	Fudan University, China	2015
High-Level Synthesis, Computational Genomics and Emerging Technologies	Invited talk in a panel	Zhejiang University, China	2015
High Design Productivity for Reliable and Energy-Efficient Circuits in the Era of Internet of Things	IEEE International Conference on ASIC	Chengdu, China	2015
Designing High-Quality Hardware on a Development Effort Budget: A Study of the Current State of High-Level Synthesis	IEEE/ACM Asia and South Pacific Design Automation Conference	Macau, China	2016
System Design Automation Techniques for FPGAs with High-Performance, Energy-Efficiency, and Reliability	Special Seminar	Toyota, San Jose	2016
Reliable and Energy-Efficient	Departmental Seminar	Peking University, China	2016

Circuit Design in the Era of Internet of Things			
New Advances on High-Level Synthesis	Departmental Seminar	Tsinghua University, China	2016
The CUDA to FPGA Compiler	ShanghaiTech Workshop on Emerging Devices, Circuits and Systems	Shanghai, China	2016
SoC, NoC and Hierarchical Bus Implementations of Applications on FPGAs Using the FCUDA Flow	IEEE Computer Society Annual Symposium on VLSI	Pittsburgh, USA	2016
System Design Automation Techniques for FPGAs with High-Performance, Energy-Efficiency, and Reliability	Special Seminar	Huawei, China	2016
The CUDA to FPGA Compiler	Workshop on FPGAs for Scientific Simulation and Data Analytics	University of Illinois, USA	2016
Automated System-Level Co-design: Are We Finally Ready?	Future Chip 2016: Challenges and Opportunities of Design Automation in China	Tsinghua University, China	2016
Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	National Taiwan University, Taiwan	2017
Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	National Tsing Hua University, Taiwan	2017
Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	National Cheng Kung University, Taiwan	2017
Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	Microsoft Research Lab, Seattle, USA	2017
Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	ShanghaiTech Workshop on Emerging Devices, Circuits and Systems (SWEDCS'2017)	ShanghaiTech University, China	2017
Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	ICC Distinguished Lecture	Michigan Technological University, Michigan	2017
Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	Workshop on Challenges and Opportunities of AI Chips	Tsinghua University, China	2017
FPGA-based Smart Devices and Platforms for the AI Revolution	SingularityU Warsaw Chapter Conference and Masters & Robots Conference	Warsaw, Poland	2017
Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	Special Seminar	Bitmain Inc., China	2017
Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	Huawei-Illinois Workshop	Champaign, IL	2017

Machine Learning on FPGAs to Face the IoT Revolution	International Conference on Computer-Aided Design (ICCAD'17)	Irvine, CA	2017
Machine Learning on FPGAs to Face the IoT Revolution	Future Chips 2017 – Smart Chips, Smart World	Tsinghua U, Beijing	2017
AI Chip for Smart Sound	SV Connect Conference	Santa Clara, CA	2018
Deep Learning for Better Variant Calling for Cancer Diagnosis and Treatment	ASPDAC'18	Jeju Island, Korea	2018
New Algorithms and Hardware Acceleration for the IoT Revolution	Special Seminar	Stanford University, CA	2018
New Algorithms and Hardware Acceleration for the IoT Revolution	ChinaDA 2018 Conference	Peking University, China	2018
New Algorithms and Hardware Acceleration for the IoT Revolution	Special Seminar	Beihang University, China	2018
New Algorithms and Hardware Acceleration for the IoT Revolution	Departmental Seminar	Southeast University, China	2018
New Algorithms and Hardware Acceleration for the IoT Revolution	Special Seminar	Anlogic, Inc., China	2018
Cognitive Computing on Large FPGA Networks	Workshop on ZJU-UIUC joint collaboration	International Campus, Zhejiang University, China	2018
Overcoming Challenges of Accelerating Deep Neural Network Computations	Plenary Talk	IEEE Computer Society Annual Symposium on VLSI, Hong Kong	2018
Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	HC Torng Lecture	Cornell University	2018
Design Productivity, Compilation, and Acceleration for Data Analytic Applications	Keynote Speech	International Conference on Big Data Analytics & Data Mining, Chicago	2018
Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Special Seminar	Beijing Institute of Technology, China	2018
Design Productivity, Compilation, and Acceleration for Data Analytic Tasks in Structural Health Monitoring	CRRC HSM Symposium	Qingdao, China	2018
Reconfigurable Software and Hardware – A New Paradigm	Future Chips, 2018	Tsinghua University, China	2018

DNNBuilder: an Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs	e-Seminar	Xilinx, Inc., USA	2018
Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Special Seminar	Yitu, Inc., Singapore	2019
Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Special Session Invited Talk, COOL Chips	Yokohama, Japan	2019