Deming Chen

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Education

B.S. Physical Chemistry	Amoy (Xiamen) University, Xiamen, China, 1990
B.S. Computer Science	University of Pittsburgh, Pittsburgh, 1995
M.S. Computer Science	University of California, Los Angeles, 2001
Ph.D. Computer Science	University of California, Los Angeles, 2005

Current and Previous Academic Positions

Mar. 2020 – present	Abel Bliss Professor of Engineering
Aug. 2015 – Feb. 2020	Professor, Donald Biggar Willett Faculty Scholar
Aug. 2011 – 2015	Associate Professor
Aug. 2005 – 2011	Assistant Professor Department of Electrical and Computer Engineering (ECE) University of Illinois, Urbana-Champaign (UIUC)
Aug. 2015 – present	Affiliate Professor (0%)
Aug. 2011 – 2015	Affiliate Associate Professor (0%)
Aug. 2008 – 2011	Affiliate Assistant Professor (0%) Coordinated Science Laboratory (CSL) Computer Science Department (CS) Information Trust Institute (ITI) University of Illinois, Urbana-Champaign (UIUC)

Other Professional Experiences

Jun. 2016 – present	Chairman, President, Co-founder, Inspirit IoT, Inc. Champaign, Illinois
Mar. 2001 – Jul. 2002	Software Engineer, Aplus Design Technologies, Inc. Los Angeles, California
Jul. 1995 – Sep. 1999	System Software Engineer, Applied Systems Associates, Inc. Murrysville, Pennsylvania
Sep. 1990 – Sep. 1991	Research Staff, Institute of Coal Chemistry Chinese Academy of Sciences, China

Visiting or Seconded Positions

Jul. 2012 – Sep. 2012	Visiting Associate Professor Center for Energy-Efficient Computing and Applications Peking University, China
Oct. 2012 – Dec. 2012	Visiting Associate Professor Department of Electrical Engineering Stanford University, USA
Mar. 2010 – Present	Seconded Faculty Appointment ARCS, Illinois Advanced Research Center at Singapore

A Summary

Deming Chen has published more than 270 journal or conference papers, and books or book chapters in the areas of reconfigurable computing, machine learning and applications, EDA, and hardware security. In recent years, he also actively pursued other research directions such as hybrid cloud and bioinformatics. He has given more than 150 invited talks sharing these research results worldwide. His research has generated high impact, with **open-sourced solutions widely adopted by both academia and industry** (e.g., FCUDA, DNNBuilder, ScaleHLS). For example, the open-source code of ScaleHLS (HPCA'22) and its follow-up works (e.g., ASPLOS'24) has been downloaded for **>3000 times** since 2022. He has received **10 Best Paper Awards**, **an ACM/SIGDA TCFPGA Hall of Fame** paper award, a few Best Poster Awards, and numerous other research, design competition, and service-related awards.

One of his representative works is a novel approach for accelerator design for energy-efficient SoCs based on a collaborative effort with Intel researchers. Through collaboration with IBM researchers, he led another project to create a new automated flow that could take arbitrary DNN (deep neural network) models and produce the most efficient FPGA implementations through a hardware generation process called *DNNBuilder*. Both works received the prestigious ***IEEE/ACM William J. McCalla ICCAD Best Paper Award*** **in 2015 and 2018**, respectively. He proposed the concept of **accelerator/DNN co-search, co-design, and co-generation** for the first time in an invited *ICSICT'18* paper, where he advocated to *"automatically generate both DNN models and their corresponding implementations as pairs"*. He then realized and demonstrated this new method through a series of papers using FPGAs as accelerators. Especially, one of the DNN models coming out of this new method, called *SkyNet*, **won double championships** in the competitive DAC System Design Contest in 2019.

He has served as PI/Co-PI on 40+ research grants administered by US funding agencies as well as industry. He has been a seconded faculty member for the Illinois ADSC center in Singapore since March 2010. He has served as an Associate Editor for several leading journals, as General Chair, Program Chair, Track/Subcommittee Chair, or TPC member for many important conferences in his research areas, and as the **Editor-in-Chief of ACM Transactions on Reconfigurable Technology and Systems** since 2019. He has rich industrial experiences. As an intern in Aplus Design Technologies, he helped commercialize his published algorithm on CPLD (complex programmable logic device) technology mapping, and the software was **exclusively licensed by Altera** (now part of Intel) and distributed to many customers worldwide. He is **one of the inventors** of the xPilot High-level Synthesis package developed at UCLA, which was licensed to AutoESL Design Technologies, Inc. Currently, he is the Co-founder, President, and Chairman of the Board for another startup company, *Inspirit IoT, Inc*.

He was the **Area Chair** for Computer Engineering during 2015-2017. During this period, the ranking of the Graduate Computer Engineering Program of UIUC reached #2 nationwide in USA. During 2020-2021, he was the **Chief Scientist** of the IBM-Illinois Center for Cognitive Computing Systems Research with an **annual budget of $3M**. Since 2021, this center was transformed into the **Hybrid Cloud & AI Thrust** within the newly formed IBM-Illinois Discovery Accelerator Institute. He then became the **Co-lead** of this Thrust. With this new role, he is co-leading and co-directing research activities of more than 40 UIUC faculty members, working with an IBM Co-lead, with an **annual budget of $3.5M**. He is also the **Director of the AMD/Xilinx Center of Excellence** since 2020, working with 23 center and external collaborative faculty members. Besides various research projects, this center built two compute clusters with FPGA and GPU accelerators, supporting about 80 users from 24 universities.

Awards and Honors

Representative Recognitions and Positions

- Abel Bliss Professor, Grainger College of Engineering, University of Illinois, 2020-present

- Director, AMD/Xilinx Center of Excellence, 2020-present
- Thrust Co-lead, Hybrid Cloud & AI Thrust, IBM-Illinois Discovery Accelerator Institute, 2021-present
- Vice President for Awards, IEEE Council on EDA, 2024-present
- Chief Scientist, IBM-Illinois Center for Cognitive Computing Systems Research, 2020-2021
- Editor-in-Chief, ACM Transactions on Reconfigurable Technology and Systems, 2019-2025
- ACM SIGDA Distinguished Service Award, 2021
- ACM Distinguished Speaker, 2019-2022
- IEEE Fellow, 2019
- Donald Biggar Willett Faculty Scholar, Grainger College of Engineering, University of Illinois, 2015-2020
- ACM SIGDA Outstanding New Faculty Award, 2010
- NSF Career Award, 2008

Best Paper Awards, Hall-of-Fame Paper Award, and Best Poster Awards

- Best Paper Award, IEEE/ACM Asia and South Pacific Design Automation Conference, 2009
- Best Paper Award, IEEE Symposium on Application Specific Processors, 2009
- Best Paper Award, IEEE International Symposium on Field-Programmable Custom Computing Machines, 2011
- Best Paper Award, Symposium on Application Accelerators in High Performance Computing, 2011
- Best Paper Award, IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2013
- Best Paper Award, IEEE/ACM International Conference on Computer-Aided Design, 2015
- Best Paper Award, IEEE/ACM International Workshop on System-Level Interconnect Prediction, 2018
- Best Paper Award, IEEE/ACM International Conference on Computer-Aided Design, 2018
- Best Paper Award, IEEE International Conference on VLSI Design, 2020
- Best Paper Award, International Conference on Intelligent Data Engineering and Automated Learning, 2021
- Induction of the "FCUDA: Enabling efficient compilation of CUDA kernels onto FPGAs" paper into the TCFPGA Hall of Fame for FPGAs, 2022
- Best Poster Award, IBM AI Horizons Colloquium, 2018
- Best Poster Award, Joint Workshop on On-Device Machine Learning & Compact Deep Neural Network Representations (ODML-CDNNR), 2019
- Best Poster Award, NSF A3D3 Institute Annual Review Meeting, 2023
- Best Poster and First Place Winner Award, DAC Ph.D. Forum, 2023
- Best Poster Award, ASPDAC, 2024

Other Paper or Research Related Recognitions or Awards

- "Power Modeling and Characteristics of Field Programmable Gate Arrays" – one of the most-downloaded articles from IEEE Transactions on CAD, 2006
- Best Paper Award Nomination, IEEE International Conference on Field-Programmable Technology, 2011
- 10-Year Retrospective Most Influential Paper Award Nomination, IEEE/ACM Asia and South Pacific Design Automation Conference, 2014
- Best Paper Candidate, IEEE/ACM International Symposium on Microarchitecture, 2018
- Honorable Mention, IEEE HPEC Graph Challenge, 2019

- Best Paper Award Nomination, IEEE/ACM Asia and South Pacific Design Automation Conference, 2021
- Best Paper Award Nomination, ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2021

Keynote and Distinguished Speech or Panels

- Keynote Speaker, IEEE International Conference on Anti-counterfeiting, Security, and Identification, 2014
- Keynote Speaker, IEEE International Conference on ASIC, 2015
- Keynote Paper, *Integration, the VLSI Journal,* 2016
- Distinguished Speaker, ICC Distinguished Lecture Series, Michigan Tech, 2017
- Distinguished Speaker, Masters & Robots Conference, 2017
- Plenary Speaker, IEEE Computer Society Annual Symposium on VLSI, 2018
- Keynote Speaker, International Conference on Big Data Analytics & Data Mining, 2018
- Distinguished Speaker, COOL Chips, 2019
- Keynote Speaker, Computing Conference, 2019
- Keynote Speaker, International Workshop on Signal Processing Systems (SiPS), 2019
- Keynote Speaker, AI Chips Summit, 2019
- Keynote Speaker, ROAD4NN: Research Open Automatic Design for Neural Networks, 2020
- Distinguished Speaker, ACM Distinguished Speaker Series, ACM Sacramento Chapter, 2020
- Keynote Speaker, ACM Great Lakes Symposium on VLSI, 2020
- Distinguished Speaker, Distinguished Speaker Series, ECE, Rice University, 2020
- Keynote Speaker, IEEE International Conference on Field-Programmable Technology, 2020
- Distinguished Speaker, ACM Distinguished Speaker Series, Universidad Católica San Pablo, Peru, 2021
- Keynote Speaker, Workshop on Reconfigurable Computing for Machine Learning – RC4ML, 2021
- Keynote Speaker, International Conference on Intelligent Data Engineering and Automated Learning, 2021
- Distinguished Speaker, Distinguished Speaker Series, ECE, Northwestern University, 2022
- Panelist, International Selection Panel of the CUHK Vice-Chancellor Early Career Professorship Scheme, 2023 and 2024

Service or Teaching Related Recognitions or Awards

- Included in the List of Teachers Ranked as Excellent, UIUC, Spring 2008 & Fall 2017
- ACM Recognition of Service Award, 2016 & 2018
- Senior Visiting Scholar, Fudan University, China, 2015-2016
- Judge, 2018 InnovateFPGA Grand Final Competition, Intel, 2018
- GLSVLSI Service Recognition Award, 2019
- Founding Chair, IEEE CEDA Central Illinois Chapter, 2016-2023
- Member, CEDA IEEE Fellow Evaluation Committee (FEC), 2021
- Chair, CEDA IEEE Fellow Evaluation Committee (FEC), 2022
- Member, ACM SIGDA Outstanding New Faculty Award Committee, 2022
- Member, ACM SIGDA Outstanding PhD Dissertation Award Committee, 2022
- Member, ACM/IEEE Design Automation Conference Best Paper Award Committee, 2023
- Chair, CEDA IEEE Fellow Evaluation Committee (FEC), 2023
- Chair, ACM SIGDA FPGA'23 Best Paper Award Committee, 2023
- Member, ACM SIGDA Outstanding New Faculty Award Committee, 2024

- Member and Cohort FEC Representative, CEDA IEEE Fellow Evaluation Committee (FEC), 2024

Other Recognitions or Competition Awards

- Achievement Award for Excellent Teamwork, Aplus Design Technologies, Inc, 2001
- Arnold O. Beckman Research Award, UIUC, 2007
- IBM Faculty Award, 2014 & 2015
- NSF SBIR (Small Business Innovation Research) Award, with Inspirit IoT, Inc., 2017
- NSF SBIR Phase II Award, with Inspirit IoT, Inc., 2018
- NSF Technology Enhancement for Commercial Partnerships (TECP) Award, with Inspirit IoT, Inc., 2019
- First Place Winner, International Hardware Design Contest on IoT, IEEE/ACM Design Automation Conference, 2017
- Third Place Winner, System Design Contest at IEEE/ACM Design Automation Conference, 2018
- First Place Winner, both the FPGA and the GPU categories, System Design Contest at IEEE/ACM Design Automation Conference, 2019
- Google Faculty Award, for supporting machine learning courses, diversity, and inclusion, 2020.
- Third Place Winner, System Design Contest at IEEE/ACM Design Automation Conference, 2020
- Member, Asian American Scholar Forum, 2021-present
- Second Place Winner, System Design Contest at IEEE/ACM Design Automation Conference, 2021

Student Fellowships or Awards Originated from Various Research Projects

- NSF Graduate Research Fellowship, 2013, 2023
- Student Best Research Award, Ph.D. Forum, IEEE/ACM Design Automation Conference, 2017
- Student Innovation Award, IEEE HPEC Graph Challenge, 2018
- Boeing Global Technology Student Recognition Award, 2018
- Google PhD Fellowship 2020
- Sundaram Seshu International Student Fellowship, 2019, 2020
- Mavis Future Faculty Fellowship, 2021
- Rambus Computer Engineering Fellowship, 2018, 2021, 2022
- A.R. Buck Knight Fellowship, 2023

Research Interests

- FPGA and reconfigurable computing
- Machine learning, AI, cognitive computing, and IoT
- System-level design and high-level synthesis
- Hybrid cloud infrastructure, energy, and security
- Hardware security and confidential computing
- Bioinformatics

Research Grants and Contracts

- Research gift, Altera, $20,000, (PI: Chen portion=**$10,000**), 2006
  Title: Novel Logic Synthesis for the New Challenges in FPGAs
- SRC, $360,000, (co-PI, Chen portion=**$180,000**), 2007-2010
  Title: Modeling, Mitigating, and Tolerating Faults due to Parameter Variation in Multicores: A Microarchitecture and CAD Approach

- Research gift, Altera, $15,000, (PI, Chen portion=**$7,500**), 2007
  Title: New Techniques in Synthesis and Physical Design for FPGAs
- NSF, $1,386,000, (co-PI, Chen portion=**$442,000**), 2007-2011
  Title: High-performance Reliable Computing: Addressing the Parameter-variation Challenge through a Cross-disciplinary Architecture, CAD, and Compiler Approach
- NSF, **$400,000**, CAREER Grant, Single PI, 2008-2013
  Title: CAREER: Nano-Centric Design Methodology for Nanoscale FPGAs
- Research gift, UIUC research board, $12,000, (co-PI, Chen portion=**$6,000**), 2008
  Title: SOS: A Nanotube-Based Configurable Logic Fabric
- Research gift, Altera, $20,000, (PI, Chen portion=**$10,000**), 2008
  Title: Novel FPGA Synthesis for Low Power
- Research gift, Sun Microsystems, **$23,000**, Single PI, 2008-2010
  Title: Reliable Circuit Design Methodology
- Intel Undergraduate Research Program (ISUR), **$3,200**, Single PI, 2009-2010
- MARCO/DARPA, Gigascale System Research Center, **$236,400**, Co-PI, 2009-2012
  Title: Parallel Programming Flow for Efficient FPGA Execution
- Internal gift fund to support PI's research at UIUC, Advanced Digital Sciences Center (ADSC), **$500,000**, Single PI, 2010-2016
  Title: GPU, Reconfigurable Computing, and High-level Synthesis for Application Acceleration
- ADSC/Singapore, **$1.3M**, Grant to support research within ADSC, PI, 2010-2013
  Title: Accelerating Immersive Remote Reality Using FPGAs and GPUs
- Research gift, Intel, **$25,000,** Single PI, 2012-2013
  Title: High-Level Synthesis for Accelerator Evaluation and Generation
- UIUC IN^3 (Interdisciplinary Innovation Initiative) fund, Office of the Vice Chancellor for Research/Liberal Arts & Sciences, $200,000, (one of 7 PIs, Chen portion=**$22,000**), 2012-2014
  Title: Developing an Interdisciplinary Research Program in Cancer Genomics
- NSF/SRC, $350,000, (PI, Chen portion=**$175,000**), 2013-2016
  Title: Collaborative Research: From High-level Synthesis to Layout: a Cross-layer Methodology for Large-scale Reliable IC Design
- SRC/DARPA, Center for Future Architectures Research (C_FAR), **$450,000**, co-PI, 2013-2015
  Title: Scalable Synthesis, Exploring Emerging Technologies for Accelerators, and Mapping Diverse Software to Heterogeneous Architectures
- Intel, **$300,000**, Single PI, 2013-2016
  Title: Customized Polyhedral Compilation for Low-Power High-Level SoC Synthesis
- ADSC/Singapore, **$1.4M**, Grant to support research within ADSC, PI, 2013-2016
  Title: Next-Generation Compilers and Architectures for Computation Acceleration with Energy Efficiency
- Research gift, IBM, **$75,000**, Faculty Award, 2014, 2015
  Title: DNA Data Error Correction and Compression with IBM Power8 System
- NSF, **$120,000** as the Graduate Research Fellowship given to a graduate student, 2013-2016
  Title: NSF Graduate Research Fellowship for Research on Hardware Security
- NSF, Research Fellowship for a graduate student (equivalent to one RA support), 2014-2015
  Title: CompGen Fellowship for DNA Error Correction and Genome Mapping
- SRC, $390,000, PI (Chen portion=**$165,000**), 2014-2017
  Title: A New Modular and Global High-level Synthesis Engine for Rapid Post-Silicon Validation of Customized Hardware and Accelerators
- NIH, **$1.3M**, co-PI (one of six), 2015-2018
  Title: Genomic Compression: From Information Theory to Parallel Algorithms
- Research gift, Jump Trading, **$105,000**, Single PI, 2015-2017

Title: Novel Architecture and Machine Learning Studies

- Research grant, Boeing, **$80,000,** Single PI, 2017-2018.
  Title: Object Recognition and Tracking for UAVs with Embedded FPGAs and GPUs
- IBM, C3SR Center, Co-PI (Chen portion=**$1.35M**), 2016-2021.
  Title: System and Acceleration for Cognitive Computing and Artificial Intelligence
- NSF and industrial partners, CCBGM Center, **$130,000**, Co-PI, 2017-2020
  Title: Improving Cancer Variant Calling through Deep Learning
- SRC, $210,000, PI (Chen portion=**$120,000**), 2018-2021
  Title: MegaBrain: Enabling Earth-scale FPGA Networks for Cognitive Computing
- ADSC/Singapore, the new CREATE center funded by NRF of Singapore, **$15M**, Co-PI (one of seven), 2017-2022.
  Title: Secure Computation Systems Design in the Smart Grid with FPGAs
- DARPA, $4.5M, Co-PI (Chen portion=**$500K**), 2018-2021
  Title: DDARING: Dynamic Data-Aware Reconfiguration, INtegration and Generation
- ZJU-UIUC Research Program, **$75,000**, Single PI, 2018-2019
  Title: Cognitive Computing on Large FPGA Networks
- Research gift, XMotors.ai, **$190,000**, PI (Chen portion=**$80,000**), 2019-2020
  Title: Machine Learning Algorithm Design and Acceleration for Autonomous Driving Cars
- Laboratory for Physical Sciences (LPS), **$300,000**, Single PI, 2020
  Title: New High-level Synthesis Techniques
- Research gift, Xilinx, **$1,080,000 gift grant + in kind gift** of hardware and software donations, Xilinx Center of Excellence, Director, 2020-2023
- NSF, **$250,000**, Planning Grant, Co-PI, 2020-2021
  Title: PPoSS: Planning: Inflight Analytics to Control Large-Scale Heterogeneous Systems
- Laboratory for Physical Sciences (LPS), **$305,000**, Single PI, 2021-2022
  Title: Advanced System-Level Design and Synthesis for FPGAs
- FIT, C-Nice Center, **$387,000**, Single PI, 2021-2023
  Title: YouHome: a Cognitive Solution to Let Your Smart Home Know You Better
- NSF, **$15M**, NSF institute, Co-PI of UIUC, (Chen portion=**$600,000**), 2022-2027
  Title: Institute for Accelerated AI Algorithms for Data-Driven Discovery (A3D3)
- IBM-Illinois Discovery Accelerator Institute (IIDAI), Co-PI, (Chen portion=**$395,000**), 2021-2023
  Project 1: A secure, Smart, and Open Hybrid Cloud System with a Software-Defined Infrastructure
  Project 2: Renewable Energy-Aware AI Workloads and their Modeling, Optimization and Resource Management in Hybrid Clouds
- GCoE, Grainger Small Equipment Grant, PI, **$139,999**, 2022
  Title: A Novel Hybrid-Cloud Computing Testbed with Green Energy
- SRC, **$285,000**, Single PI, 2023-2025
  Title: vHLS: Verifiable High-level Synthesis
- HPE, **$164,000**, Co-PI, 2023-2024
  Title: Language, Compiler, and Runtime System for the Dot Product Engine
- NSF CITES center, **$61,500,** Co-PI, 2023-2024
  Title: Application of DPU Accelerators to the Process Layer Security
- ADSC/Singapore, CREATE center funded by NRF of Singapore, **$25M**, Thrust Lead, 2023-2028.
- IBM-Illinois Discovery Accelerator Institute (IIDAI), Co-PI and PI respectively, 2023-2025
  Project 1: Sustainable AI Hybrid Cloud Systems Powered by Renewable Energy and Smart Grid (**$338K**)
  Project 2: Confidential Computing with Heterogeneous Accelerators in Hybrid Clouds (**$151K**)

Teaching Experiences and Contributions

- Fall 2003/2004, Teaching Assistant, CS 258G: Logic Synthesis of Digital Systems, University of California, Los Angeles
- Spring 2008/2009/2010, ECE 412: Microcomputer Laboratory
- Spring 2006/2007/2009, Fall/2016, ECE 425: Introduction to VLSI System Design
- Fall 2006/2007, ECE 598BL: Design and Synthesis of System-on-Chip (new course developed)
- Fall 2008/2009/2010/2011/2013/2015/2017/2018/2020/2021/2022/2023, ECE 527: System-on-Chip Design (permanent version of ECE 598BL)
- Fall 2011/Spring 2019, ECE 411: Computer Organization and Design
- Fall 2013/Spring 2014, ECE 298: Digital System Design Laboratory (new course developed). This course became the new ECE 385 course in Fall 2014, which is a required course for all ECE undergraduate students.
- Fall 2014, Spring 2012/2013/2016/2017, ECE 385: Digital Systems Laboratory
- Spring 2018, ECE 462: Logic Synthesis
- Spring 2019/2020/2021, ECE 498ICC: IoT and Cognitive Computing (new course co-developed)
- Spring 2023/2024, ECE 479: IoT and Cognitive Computing (permanent version of the ECE 498ICC course)

Patents and Licenses

- U.S. Patent Application No.: 18/328,716. Filing date: June 2023.
  Co-inventors: Bharat Sukhwani, Martin Ohmacht, Hubertus Franke, Sameh Asaad, Scott Smith, Deming Chen
  Title: "Dynamic Assignment of Device Queues to Virtual Functions to Provide to Virtual Machines"
- U.S. Patent No.: 11,706,163. Issue date: July 2023.
  Co-inventors: Jian Huang, Deming Chen, Alexander Gerhard Schwing, Youjie Li.
  Title: "Accelerating Distributed Reinforcement Learning with In-switch Computing".
- U.S. Patent No.: 3304111. Issue date: Mar 11, 2020.
  Co-inventors: Keith A. Campbell, Hai Lin, Deming Chen, Subhasish Mitra.
  Title: "System-Level Validation of Systems-On-A-Chip (SOC)".
- Technology license: a company licensed the "Low Loss DNN Quantization Software" out of ADSC/UIUC in 2021.
  Co-inventors: Yao Chen, Deming Chen, Cong Hao
- Technology license: AutoESL Inc. licensed the xPilot technology out of UCLA, 2006.
  Co-inventors: Deming Chen, Jason Cong, Yiping Fan, Guoling Han, Wei Jiang, and Zhiru Zhang.
  Title: "xPilot: A Platform-Based Behavioral Synthesis System".
  This technology eventually led to the acquisition of AutoESL by Xilinx. xPilot became the high-level synthesis engine of Xilinx Vivado HLS (high-level synthesis).
- Technology license: Inspirit IoT, Inc. licensed the VAST HLS technology out of ADSC/UIUC, 2016.
  Co-inventors: Deming Chen, Hongbin Zheng, Kyle Rupnow, Swathi Gurumani.
  Title: "VAST: High-level Synthesis Tool".
- Technology license: a company licensed the RASP technology out of UCLA, 2017.
  Co-inventors: Deming Chen, Jason Cong, Eugene Ding, Zhijun Huang, Yeanyow Hwang, Chang Wu, Sarah Xu.
  Title: "RASP: FPGA/CPLD Technology Mapping and Synthesis Package".

Hardware Donations

- Equipment grant, Intel, equivalent to $20,000, 2005
- FPGA boards (30 DE2 boards, two DE3 boards, and one DE5 board), Altera, equivalent to $28,000, 2006, 2009, 2013
- TRDB_DC2 1.3Mega Pixel Digital Camera Module (30 items), Altera, equivalent to $2,100, 2006.
- FPGA boards (one Virtex-5 board, 25 Zedboards, and one high-end Virtex-7 board), Xilinx, equivalent to $19,000, 2009, 2013, 2014
- 260 DE2-115 FPGA boards, Altera, equivalent to commercial value of $130,000, to be used in ECE 385, the new course version developed, 2014, 2015, 2016
- Altera Arria 10 board, equivalent to $4,000, 2016.
- Xilinx Virtex UltraScale+ board, equivalent to $6,995, 2017.
- Xilinx, two V7-VC709-G boards, equivalent to $10,000, 2017.
- Xilinx, Zynq UltraScale+ MPSoC ZCU102, equivalent to $2,500, 2018
- Intel, Arria 10 SoC, equivalent to $4,500, 2018
- Xilinx, 14 high-end FPGA donations to support Xilinx Center of Excellence and Xilinx Adaptive Compute Clusters (XACC) at UIUC, equivalent to $80K, 2020, 2021
- Xilinx, 40 Pynq Z2 and 10 Ultra96-V2 boards to support ECE 527 SoC Design, 2020
- Xilinx, four Alveo SN1000 SmartNiC cards and one VCK5000 Versal board, equivalent to $12,325, 2021, 2022
- AMD, 6 Xilinx Alveo U55C boards and 6 Xilinx VCK5000 boards, equivalent to $42,840, 2022.
- AMD, three Heterogeneous Accelerated Compute nodes (each with 2 EPYC Milan processors and 4 MI210 Instinct GPU boards), equivalent to $180K, 2023.
- AMD, Ryzen AI Mini-PC and Laptop, equivalent to $2000, 2024.

Software Donations and Instruction Grants

- Software donation, Microsoft
- Quartus II design environment and Nios II embedded soft processors (30 licenses), Altera
- Xilinx Vivado Design Suite (50 licenses), Xilinx
- UIUC SIIP (Strategic Instructional Initiatives Program) fund, UIUC College of Engineering, one of 16 PIs, $125,000 for the first year, 2012-2015
- Various Xilinx IPs, including 100G Ethernet IPs and NVMe IPs, 2020
- Google Faculty Award, $10,000, for supporting ECE 498 ICC: IoT and Cognitive Computing, 2020

Student and Postdoc Advising

Current Graduate Students:

(*Ph.D. Candidate* indicates passing of either the Ph.D. qualifying exam or the Ph.D. prelim exam.**)**

- Kaiwen Cao (Ph.D. candidate)
- Zutai Chen (M.S. student)
- Bill Dai (M.S. student)
- Yingbing (Wendy) Huang (Ph.D. student)
- Paul Jeong (Ph.D. candidate)
- Manvi Jha (Ph.D. student)
- Gregory Jun (Ph.D. candidate)
- William Kozlowski (M.S. student)
- Soyeon Lee (Ph.D. student)

- Jason Leung (M.S. student)
- Yuhong Li (Ph.D. candidate)
- Weihang Long (Ph.D. student)
- Junhao Pan (Ph.D. candidate)
- Sanjana Pingali (M.S. student)
- Wei Ren (Ph.D. candidate)
- Haochen Shen (M.S. student)
- Scott Smith (Ph.D. candidate)
- Jiaxin Wan (Ph.D. candidate)
- Jinghua Wang (Ph.D. candidate)
- Hanchen Ye (Ph.D. candidate)
- Selin Yildirim (Ph.D. student)
- Neo (Zehua) Yuan (Ph.D. candidate)
- Tim (Jialiang) Zhang (Ph.D. candidate)
- Tianxiang Zheng (M.S. student)

Current Researchers at Illinois ARCS at Singapore (formerly ADSC):

- Debasish Mukherjee (Postdoc Researcher)
- Shiqing Li (Postdoc Researcher)

Current Undergraduate Researchers:

- Suleiman Alkhateeb
- Cain Gonzalez
- Jintong Hou
- Muhammad Khan
- Marissa Lanz
- Omolola Okesanjo

Alumni from UIUC:

Postdocs

- Cong (Callie) Hao, 2017-2020 (joined Georgia Institute of Technology, Assistant Professor)

Ph.D. Graduates

- Lei Cheng, Ph.D., 2007 (co-advised with Prof. Martin Wong; joined Synplicity)
- Chen Dong, Ph.D., 2010 (joined Magma; now Synopsys)
- Lu Wan, Ph.D., 2012 (joined Tensilica; now Cadence)
- Alex Papakonstantinou, Ph.D., 2012 (joined NVIDIA)
- Yun Heo, Ph.D., 2015 (joined Samsung)
- Ying-Yu Chen, Ph.D., 2015 (joined Synopsys)
- Sven Choden Konigsmark, Ph.D., 2017 (co-advised with Prof. Martin Wong; joined Google)
- Keith Campbell, Ph.D., 2017 (joined Inspirit IoT)
- Chen-Hsuan Lin, Ph.D., 2018 (joined Google)
- Di He, Ph.D., 2019 (joined Amazon)
- Yi Liang, Ph.D., 2019 (joined Google)
- Ashutosh Dhar, Ph.D., 2021 (joined NVIDIA)
- Sitao Huang, Ph.D., 2021 (co-advised with Prof. Wen-Mei Hwu; joined UC-Irvine as an assistant professor)
- Xinheng Liu, Ph.D., 2022 (joined Synopsys)

- Xiaofan Zhang, Ph.D., 2022 (joined Google)
- Anand Ramachandran, Ph.D., 2023 (joined Amazon)
- Wei Zuo, Ph.D., 2023 (joined Microsoft)

M.S. Graduates

- Shoaib Akram, M.S., 2009 (joined Institute of Computer Science, Foundation for Research and Technology, Greece, and later joined Australian National University as an assistant professor.)
- Scott Cromar, M.S., 2009 (joined law school, UIUC)
- Scott Chilstedt, M.S., 2010 (joined IBM)
- Greg Lucas, M.S., 2010 (joined Intel)
- Chi-Chen Peng, M.S., 2010 (joined Springsoft; now Synopsys)
- Artem Rogachev, M.S., 2012 (joined TI)
- Jacob Tolar, M.S., 2013 (joined Yahoo)
- Chong Li, M.S., 2013 (joined University of Washington as a Ph.D. student)
- Amit Sangai, M.S., 2013 (joined law school, India)
- Chunan Wei, M.S., 2014 (joined Qualcomm)
- Ying Chen, M.S., 2015 (joined Google)
- Pranay Vissa, M.S., 2015 (joined a startup in silicon valley and then Amazon)
- Warren Kemmerer, M.S., 2016 (joined Intel)
- Yan Yan, M.S., 2016 (joined Google)
- Zelei Sun, M.S., 2016 (joined Google)
- Daniel Chen, M.S., 2017 (joined a startup in silicon valley)
- Gowthami Manikandan, M.S., 2017 (joined Apple)
- Chuanhao Zhuge, M.S., 2017 (joined Apple)
- Zhangqi Xu, M.S., 2018 (joined a startup in silicon valley)
- Huiren Li, M.S., 2018 (joined Amazon)
- Kenny Umenthum, M.S., 2019 (joined TI)
- Jong Bin Lim, M.S., 2019 (joined NovuMind)
- Dae Hee Kim, M.S., 2019 (joined a startup in Pittsburgh)
- Xingkai Zhou, M.S., 2020 (joined NVIDIA)
- Qin Li, M.S., 2020 (joined Apple)
- Zhijie Jin, M.S., 2020 (joined a startup company in China)
- Yujia Qiu, M.S., 2020 (joined NVIDIA)
- Jack Li, M.S., 2021 (joined Qualcomm)
- Mang Yu, M.S., 2021 (joined NVIDIA)
- Paul Reckamp, M.S., 2022 (joined Apple)
- Vibhakar Vemulapati, M.S., 2022 (joined Apple)
- Curtis Yu, M.S., 2023 (joined NVIDIA)
- Yizhen Lu, M.S., 2023 (joined NVIDIA)
- Meghna Mandava, M.S., 2023 (joined AMD)
- Sean Amin Farhat-Sabet, M.S., 2023 (joined NVIDIA)

- **Undergraduate Researcher Alumni:**
  Bryan Clodfelter, Jaeho Lee, Kyungmin Lee, Allyson Moisan, Andrew Ryan, Alexander Uribe, Yohannes Kifle, Christine Lee, Wenxun Huang, Artem Rogachev, Shuotao Xu, Sai Ma, Chunan Wei, Tielong Su, Liana Nicklaus, Daniel Chen, Chuanhao Zhuge, Xinheng Liu, George Li, Huiren Li, Dae Hee Kim, Kenny Umenthum, Luis Pabon, Wei-You Chen, Leon He, Nitesh Neupane, Zizhen Liu, Yikuan Chen, Qin Li, Yujia Qiu, Mang Yu, Yangyang Yu, etc.

Many of them either joined top graduate schools (such as MIT, Berkeley, Harvard, CMU, Columbia, and UIUC) or high-tech companies (such as Microsoft, ARM, and TI).

Alumni from Illinois ARCS (formerly ADSC):

- Dr. Yao Chen, postdoc researcher & senior scientist, ADSC, 2019-2022. Now Research Assistant Professor at National University of Singapore (NUS).
- Dr. Yun (Eric) Liang, postdoc researcher, ADSC, 2010-2012. Now Associate Professor at Peking University, China.
- Dr. Gabriel Noaje, postdoc researcher, ADSC, 2013-2014. Now at NVidia.
- Dr. Swathi Gurumani, postdoc researcher & principal research engineer, ADSC, 2012-2016. Now at MulticoreWare.
- Dr. Kyle Rupnow, postdoc researcher & senior scientist, ADSC, 2010-2016. Now at Google.
- Dr. Liwei Yang, senior research engineer, ADSC, 2016-2017. Now at IHPC.
- Dr. Hongbin Zheng, senior software engineer, ADSC, 2012-2015. Now at Amazon.
- Mr. Prakhar Ganesh, research engineer, ADSC, 2019-2021. Now a grad student at NUS.
- Mr. Mohammad Ali Khan, software engineer, ADSC, 2019-2020. Now a grad student at UCSD.
- Mr. Tan Nguyen, software engineer, ADSC, 2015-2017. Now a Ph.D. student at UC Berkeley.
- Mr. Muhammad T. Satria, software engineer, ADSC, 2012-2014. Now at National Supercomputing Centre, Singapore.
- Ms. Zheng Cui, software engineer, ADSC, 2011-2012.
- Mr. Yinan Li, software engineer, ADSC, 2010-2012.

Publications

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Conference (HPEC), September 2018. **(Student Innovation Award)**

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[133] Anand Ramachandran, Eric Klee, Steven Lumetta, and Deming Chen, "A Recurrent Markov State-space Generative Model for Sequences," *Proceedings of International Conference on Artificial Intelligence and Statistics*, Apr. 2019.

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[140] Yao Chen, Kai Zhang, Cheng Gong, Cong Hao, Xiaofan Zhang, Tao Li, and Deming Chen, "T-DLA: An Open-source Deep Learning Accelerator for Ternarized DNN Models on Embedded FPGA," *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, July 2019.

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[145] Sitao Huang, Deming Chen, and Wen-Mei Hwu, "Accelerating Sparse Deep Neural Network on FPGA," *Proceedings of IEEE High Performance Extreme Computing Conference (HPEC)*, September 2019. **(Honorable Mention)**

[146] Cong Hao, Atif Sarwari, Zhijie Jin, Husam Abu-Haimed, Daryl Sew, Yuhong Li, Xinheng Liu, Bryan Wu, Dongdong Fu, Junli Gu, and Deming Chen, "A Hybrid GPU + FPGA System Design for Autonomous Driving Cars," *Proceedings of IEEE International Workshop on Signal Processing Systems*, October 2019. **(Invited)**

[147] Cong Hao, Yao Chen, Xinheng Liu, Atif Sarwari, Daryl Sew, Ashutosh Dhar, Bryan Wu, Dongdong Fu, Jinjun Xiong, Wen-mei Hwu, Junli Gu, and Deming Chen, "NAIS: Neural Architecture and Implementation Search and its Applications in Autonomous Driving," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2019. **(Invited)**

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[149] Dae Hee Kim, Rakesh Nagi, and Deming Chen, "Thanos: High-Performance CPU-GPU Based Graph Partitioning Using Cross-Decomposition," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2020.

[150] Ashutosh Dhar, Mang Yu, Wei Zuo, Xiaohao Wang, Nam Sung Kim, and Deming Chen, "Leveraging Dynamic Partial Reconfiguration with Scalable ILP Based Task Scheduling," *Proceedings of IEEE International Conference on VLSI Design*, January 2020. (**Best Paper Award**)

[151] Xinyu Chen, Yao Chen, Ronak Bajaj, Jiong He, Bingsheng He, Weng-Fai Wong, and Deming Chen, "Is FPGA Useful for Hash Joins?", *Proceedings of Conference on Innovative Data Systems Research (CIDR)*, January 2020.

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[170] Cong Hao and Deming Chen, "Software/Hardware Co-design for Multimodal Multi-task Learning in Autonomous Systems", *Proceedings of IEEE International Conference on Artificial Intelligence Circuits and Systems*, June 2021. (**Invited**)

[171] Hyunmin Jeong and Deming Chen, "TwinDNN: A Tale of Two Deep Neural Networks", *Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors*, July 2021.

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[181] Wei Ren, Junhao Pan, and Deming Chen, "AccGuard: Secure and Trusted Computation on Remote FPGA Accelerators", *Proceedings of IEEE International Symposium on Smart Electronic Systems*, December 2021.

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[183] Prakhar Ganesh, Yao Chen, Yin Yang, Deming Chen, and Marianne Winslett, "YOLO-ReT: Towards High Accuracy Real-time Object Detection on Edge GPUs", *Proceedings of Winter Conference on Applications of Computer Vision*, January 2022.

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[185] Hanchen Ye, Gregory Jun, Hyunmin Jeong, Stephen Neuendorffer, and Deming Chen, "Invited: ScaleHLS, a Scalable High-level Synthesis Framework with Multi-level Transformations and Optimizations," *Proceedings of IEEE/ACM Design Automation Conference*, July 2022. (**Invited**)

[186] Edward Richter and Deming Chen, "Qilin: Enabling Performance Analysis and Optimization of Shared-Virtual Memory Systems with FPGA Accelerators," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, November 2022.

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[191] Hanchen Ye, Hyegang Jun, Jin Yang, and Deming Chen "High-level Synthesis for Domain Specific Computing," *Proceedings of International Symposium on Physical Design*, March 2023. (**Invited**)

[192] Yuhong Li, Tianle Cai, Yi Zhang, Deming Chen, and Debadeepta Dey, "What Makes Convolutional Models Great on Long Sequence Modeling?" *Proceedings of International Conference on Learning Representations*, May 2023.

[193] Meghna Mandava, Paul Reckamp, and Deming Chen, "Nimblock: Scheduling for Fine-grained FPGA Sharing through Virtualization," *Proceedings of International Symposium on Computer Architecture*, June 2023.

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[195] Deming Chen, "Lightning Talk: The Next Wave of High-level Synthesis," *Proceedings of ACM/IEEE Design Automation Conference*, July 2023. (**Invited**)

[196] Luyang Yu, Yizhen Lu, Meghna Mandava, Edward Richter, Vikram Sharma Mailthody, Seung Won Min, Wen-Mei Hwu, and Deming Chen, "FSSD: FPGA-based Emulator for SSDs," *Proceedings of the International Conference on Field-Programmable Logic and Applications*, September 2023.

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[198] Benjamin Reidys, Yuqi Xue, Yiqi Liu, Daixuan Li, Bharat Sukhwani, Wen-mei Hwu, Deming Chen, Sameh Asaad, and Jian Huang, "RackBlox: A Software-Defined Rack-Scale Storage System with Network-Storage Co-Design," *Proceedings of the Symposium on Operating Systems Principles*, October 2023.

[199] Yizhen Lu, Curtis Yu, and Deming Chen, "SSDe: FPGA-based SSD Express Emulation Framework," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, October 2023.

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[201] Lily Jiaxin Wan, Yingbing Huang, Yuhong Li, Hanchen Ye, Jinghua Wang, Xiaofan Zhang, and Deming Chen, "Invited: Software/Hardware Co-design for LLM and Its Application for Design Verification," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2024. (**Invited**)

[202] Hanchen Ye, David Pan, Chris Leary, Deming Chen, and Xiaoqing Xu, "Subgraph Extraction-based Feedback-guided Iterative Scheduling for HLS", *Proceedings of the Conference on Design, Automation & Test in Europe (DATE)*, March 2024.

[203] Hanchen Ye, Hyegang Jun, and Deming Chen, "HIDA: A Hierarchical Dataflow Compiler for High-Level Synthesis", *Proceedings of ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2024.

[204] Hongpeng Guo, Haotian Gu, Xiaoyang Wang, Bo Chen, Eun Kyung Lee, Tamar Eilam, Deming Chen, and Klara Nahrstedt, "FedCore: Straggler-Free Federated Learning with Distributed Coresets", *Proceedings of IEEE International Conference on Communications (ICC): IoT and Sensor Networks Symposium*, June 2024.

Other Workshop Papers, Poster Papers, or Online Publications
(Most of these papers/posters were accepted through a reviewing process.)

[1] C. Dong, S. Chilstedt, and D. Chen, "Variation Aware Routing for Three-Dimensional FPGAs," *Workshop on 3D Integration and Interconnect-Centric Architectures*, Feb. 2009. (A later version with the same title appeared in *IEEE Computer Society Annual Symposium on VLSI*, May 2009.)

[2] A. Papakonstantinou, K. Gururaj, J. Stratton, D. Chen, J. Cong, and W.M. Hwu, "High-Performance CUDA Kernel Execution on FPGAs," *International Conference on Supercomputing*, June 2009. (Two-page extended abstract in the proceeding.)

[3] D. Chen, S. Chilstedt, C. Dong, and E. Pop, "What Everyone Needs to Know about Carbon-Based Nanocircuits," *Online Knowledge Center, Topic: Back-End, Sub-topic: New Technologies and Directions, IEEE/ACM Design Automation Conference*, 2010. (**Invited**)

[4] L. Wan and D. Chen, "Circuit Level Dynamic Behavior Analysis through Timed Ternary Decision Diagram," *Proceedings of IEEE/ACM International Workshop on Logic & Synthesis*, June 2010.

[5] K. Rupnow, Y. Liang, D. Min, M. Do and D. Chen, "Mobile 3D Vision - Algorithm and Platform Challenges," *FPL Workshop on Computer Vision on Low-Power Reconfigurable Architectures*, 2011.

[6] Y-Y. Chen, A. Rogachev, A. Sangai, G. Iannaccone, G. Fiori, and D. Chen, "A SPICE-compatible Model of Graphene Nano-Ribbon Field-Effect Transistors", *NSF Workshop on Nano and Micro Manufacturing*, May 2013.

[7] Y-Y Chen, A. Sangai, M. Gholipour, and D. Chen, "Effects of Process Variation on the Circuit-Level Performance of Graphene Nano-Ribbon Field-Effect Transistors," *Workshop on Variability Modeling and Characterization*, Nov. 2013.

[8] A. Dhar and D. Chen, "Neuromorphic Architecture Inspired Fast, Efficient and Configurable On-Chip Learning Via In-Memory Computing and RRAM", Poster paper, *2015 Workshop on Hardware and Algorithms for Learning On-a-chip (HALO)*, Nov. 2015.

[9] D. Chen, J. Cong, S. Gurumani, W.M. Hwu, K. Rupnow, and Z. Zhang, "System Synthesis and Automated Verification: Design Demands for IoT Devices," *Sensors to Cloud Architectures Workshop*, March 2016.

[10] Di He, Boon Pang Lim, Xuesong Yang, Mark Hasegawa-Johnson, and Deming Chen, "Selecting frames for automatic speech recognition based on acoustic landmarks," *The Journal of the Acoustical Society of America*, 141(5):3468-3468, May 2017. DOI: 10.1121/1.4987204.

[11] Xiaofan Zhang, Mohamed El Hadedy, Wen-mei Hwu, Nam Sung Kim, Jinjun Xiong, and Deming Chen, "Implementing Long-term Recurrent Convolutional Network Using HLS on POWER System," *IBM OpenPOWER Summit*, Las Vegas, 2018.

[12] Junsong Wang, Qiuwen Lou, Xiaofan Zhang, Chao Zhu, Yonghua Lin, and Deming Chen, "A Design Flow of Accelerating Hybrid Extremely Low Bit-width Neural Network in Embedded FPGA," *Design Automation Conference (DAC) Late Breaking Results*, San Francisco, 2018.

[13] Xiaofan Zhang, Hao Cong, Yuhong Li, Yao Chen, Jinjun Xiong, Wen-Mei Hwu, and Deming Chen, "A Bi-Directional Co-Design Approach to Enable Deep Learning on IoT Devices," *Joint Workshop on On-Device Machine Learning & Compact Deep Neural Network Representations, ICML 2019 Workshop*, June 2019.

[14] Cong Hao, Xinheng Liu, and Deming Chen, "An FPGA/DNN Co-design Methodology," *Poster at SRC TECHCON*, September 2019.

[15] Sitao Huang, Kun Wu, Paul Jeong, Chengyue Wang, Deming Chen, and Wen-mei Hwu, "PyLog: An Algorithm-Centric Python-Based FPGA Programming and Synthesis Flow", *Poster at ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2021.

[16] Hanchen Ye, Cong Hao, Hyunmin Jeong, Jack Huang, and Deming Chen, "ScaleHLS: Achieving Scalable High-Level Synthesis through MLIR", *ASPLOS Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE21)*, April 2021.

[17] Xiaofan Zhang, Hanchen Ye, and Deming Chen, "Being-ahead: Benchmarking and Exploring Accelerators for Hardware-Efficient AI Deployment", *MLSys Workshop on Benchmarking Machine Learning Workloads on Emerging Hardware (MLBench21)*, April 2021.

[18] Philip Harris, Erik Katsavounidis, William Patrick McCormack, Dylan Rankin, Yongbin Feng, Abhijith Gandrakota, Christian Herwig, Burt Holzman, Kevin Pedro, Nhan Tran, Tingjun Yang, Jennifer Ngadiuba, Michael Coughlin, Scott Hauck, Shih-Chieh Hsu, Elham E Khoda, Deming Chen, Mark Neubauer, Javier Duarte, Georgia Karagiorgi, and Mia Liu, "Physics Community Needs, Tools, and Resources for Machine Learning", https://arxiv.org/abs/2203.16255, March 2022. (Contribution to Snowmass 2021.)

[19] Meghna Mandava and Deming Chen, "Nimblock: Scheduling for Fine-grained FPGA Sharing through Virtualization," *Poster, ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2023.

[20] Qian Jiang, Xiaofan Zhang, Deming Chen, Minh N. Do, and Raymond A. Yeh, "EH-DNAS: End-to-End Hardware-aware Differentiable Neural Architecture Search", *ICML 2023 Workshop on Differentiable Almost Everything*, July 2023.

Ph.D. Thesis

- *Design and Synthesis for Low-Power FPGAs*, Computer Science Department, University of California at Los Angeles, 2005. (Ph.D. advisor: Prof. Jason Cong).

Professional Activities, Membership, and Services

Editorship:

- Editor-in-Chief, ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2019 – 2025
- Associate Editor, Frontiers in Electronics, 2021 – present
- Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2013 – 2020
- Associate Editor, IEEE Transactions on Circuits and Systems II (TCAS-II), 2016 – 2019
- Lead Guest Editor, Special Issue of *Integration, the VLSI Journal* on Hardware Acceleration for Machine Learning, 2018-2019
- Guest Editor and main contact, Special Issue of *IEEE Design & Test Magazine* on Machine Intelligence at the Edge, 2018-2019
- Associate Editor, IET Cyber-Physical Systems: Theory & Applications, 2016 – 2019
- Associate Editor, Journal of Low Power Electronics (JOLPE), 2009 – 2019
- Associate Editor, Journal of Nanotechnology: Nanomedicine & Nanobiotechnology (NTMB), 2014 – 2020
- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2012 – 2018
- Associate Editor, ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2017 – 2018 (Guest Associate Editor, 2015-2016)
- Associate Editor, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2009 – 2015
- Associate Editor, IEEE Transactions on Circuits and Systems I (TCAS-I), 2009 – 2012

- Lead Guest Editor for a special issue of Journal of Electrical and Computer Engineering on "ESL Design Methodology", 2011
- Associate Editor, Journal of Circuits, Systems and Computers (JCSC), 2009 – 2012
- Associate Editor, ACM SIGDA Electronic Newsletter, 2008 – 2010
- Associate Editor, VLSI Circuit and Semiconductor Technology Division, Translated Series on Foreign Advanced Technologies, China Machine Press, 2007

Professional Society Membership and Leadership:

- Vice President for Awards, IEEE Council on EDA, 2024-present
- IEEE, member since 2000; IEEE Circuits and Systems Society, and Computer Society
- ACM, member since 2003
- Member, The Design Automation Technical Committee (DATC)
- Co-chair, ACM SIGDA Logic/RTL Synthesis Technical Committee, 2010 – 2013
- Member, ACM SIGDA FPGA, Configurable Computing Technical Committee, 2010 – present

Service to Professional Conferences or Committees:

Various conference chair positions

- Various session chair services: ICCD 2005/2010; ASPDAC 2007/2011/2014/2020; DATE 2009; ICCAD 2007/2011/2017/2018; ISFPGA 2008/2010/2013/2014; DAC 2009/2010/2014; SLIP 2009/2010; SiPS 2019; Nano-S&T 2019; FPL 2023
- TPC Subcommittee chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2009, 2010, 2011, 2013, 2020
- TPC CAD track co-chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- TPC CAD track chair/co-chair, IEEE International Symposium on Circuits and Systems (ISCAS), 2010-2011
- TPC Track chair, IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2011
- TPC Track chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2012
- TPC Track chair, IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2012
- Finance chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2010
- Publications chair, IEEE Symposium on Application Specific Processors (SASP), 2010
- Finance chair, IEEE Symposium on Application Specific Processors (SASP), 2011
- Program chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2011
- CANDE Workshop chair, 2011
- General chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2012
- Program chair, Pacific-Rim Outlook Forum on IC Technology (PROFIT), 2012
- Publicity chair, IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2013-2015
- TPC Track chair, IEEE International Conference on Computer Design (ICCD), 2014-2016
- TPC Track chair, IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2014-2016
- Program chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2015
- General chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2016
- Program co-chair, First International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC), 2015

- Finance chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2017
- Program co-chair, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2017
- Sponsorship chair, IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2017
- General chair, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2018
- TPC Track co-chair, International Conference on VLSI Design (VLSID), 2020
- General co-chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2021
- General chair, IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2021
- Workshop chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2022
- Special Session chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023
- Technical Program Vice chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2024
- TPC Track chair, IEEE/ACM Design Automation Conference (DAC), 2024
- Founding General co-chair, the First IEEE International Workshop on LLM-Aided Design (LAD'24), June 2024

Technical program committee and conference steering committee

- ACM/SIGDA International Symposium on FPGA (FPGA), 2006-2024
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2018-2024
- International Conference on Field Programmable Logic and Applications (FPL), 2008-2019
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2007-2011, 2013-2014, 2020
- IEEE International Symposium on Circuits and Systems (ISCAS), 2007-2008, 2010-2011
- IEEE International Conference on Computer Design (ICCD), 2007-2016
- IEEE/ACM International Symposium on Quality Electronic Design (ISQED), 2009-2014
- IEEE International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2009-2011
- IEEE Reconfigurable Architectures Workshop (RAW), 2009-2010
- IEEE/ACM Design Automation Conference (DAC), 2009-2011, 2015-2018
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- IEEE Symposium on Application Specific Processors (SASP), 2009
- IEEE/ACM System Level Interconnect Prediction (SLIP), 2009-2012
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2009-2012, 2018-2019
- International Workshop on High-Performance Reconfigurable Computing Technology and Applications (HPRCTA), 2009-2010
- ACM/SIGDA Ph.D. Forum at DAC, 2007-2014
- IEEE International Conference on VLSI Design (VLSI), 2010-2011
- Design, Automation, and Test in Europe (DATE), 2010-2011
- IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2010-2016, 2018
- Workshop on Emerging Parallel Architectures (WEPA), 2011-2012
- International Workshop on Logic and Synthesis (IWLS), 2011
- IEEE International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES), 2013-2014

- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2014
- IEEE International Conference on High Performance Computing (HiPC), 2015
- International Workshop on High-performance Reconfigurable Computing (H2RC), 2015
- Steering Committee Member, IEEE/ACM System Level Interconnect Prediction (SLIP), 2012-2020
- International European Conference on Parallel and Distributed Computing (Euro-Par), 2017
- Euro-Par Advisory Board, 2017-2020
- Steering Committee member, ACM/SIGDA International Symposium on FPGA (FPGA), 2016-present
- Steering Committee member, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2018-present
- Steering Committee member, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2021-present

Special Session/Workshop/Panel organizer

- Workshop co-organizer and co-coordinator: "Grand Challenges in FPGA Research", 2007
- Panel chair and moderator: "CMOS vs. NANO: Comrades or Rivals," ACM/SIGDA International Symposium on FPGA, 2009
- Panel organizer and moderator, "Impact of Emerging Interconnect Technologies on SLIP Research Directions", IEEE/ACM System Level Interconnect Prediction (SLIP), 2009
- ACM/SIGDA 2009 University Booth Keynote Speech organizer and moderator, 2009
- Hot Topic Session co-organizer, "Memristor: Device, Design and Application", Design, Automation, and Test in Europe (DATE), 2010
- Special session organizer: "ESL Design", IEEE International Conference on ASIC (ASICON), 2011
- Special session organizer: "Would Emerging Technologies Revolutionize How We Achieve Low Power?" IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2013
- Special session organizer: "Energy Efficiency, Complexity, and High-Level Design Methodologies" IEEE International Symposium on Integrated Circuits (ISIC), 2014
- Special session organizer: "Devices, Systems, and Design Methodologies for IoT", IEEE International Conference on ASIC (ASICON), 2015
- Special session organizer: "High-Level Synthesis – Now, the Future, and the Dark Secrets", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2016
- Keynote session co-organizer: "Plenary Session in Memory of Prof. Edward J. McCluskey" IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2017
- Special session organizer: "Where Are the True Innovations and Potentials of IoT?" IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2017
- Special session organizer: "Deep Learning for Applications that Live on Big Data", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018
- Panel chair and moderator: "FPGAs in Supercomputers: Opportunity or Folly?" ACM/SIGDA International Symposium on FPGA (FPGA), 2019
- Panel organizer: "LLM-Aided Design," IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2023
- Special session organizer: "LLM Acceleration and Specialization for Circuit Design and Edge Applications", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2024

Tutorials, Short Courses, and Panelist

- Panelist: “Best ways to Use Billions of Devices on a Chip,” IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2008.
- Tutorial presenter: “Latest Advances and Future Opportunities on CAD for FPGAs,” IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2008.
- Tutorial organizer and presenter: “From Nanodevices to Nanosystems: Promises and Challenges of IC Design with Nanomaterials,” IEEE/ACM Design Automation Conference (DAC), 2009.
- Panelist: Session discussion, IEEE/ACM System Level Interconnect Prediction (SLIP), 2009, 2010.
- Dragon Star Lecture Series, Sichuan University, China, 2011.
- Tutorial organizer and presenter: “The Device-to-System Spectrum – A Tutorial on IC Design with Nanomaterials,” Design, Automation & Test in Europe (DATE), 2012.
- Short lectures: “SoC Design Methodology,” School of Information Science and Technology, Xiamen University, China, 2012.
- Tutorial co-organizer and presenter: “High-Level Synthesis for Low-Power Design,” IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2014.
- Tutorial instructor: “Bloom-filter Based DNA Error Correction and Acceleration Using FPGAs,” Workshop on Genome Assembly and Annotation, Bio IT World Conference & Expo, Boston, 2014.
- Short course and on-site training for High Level Synthesis, NVidia, 2015.
- Panelist: Bio-informatics session of the CSL Student Conference of UIUC, Feb. 2017.
- Short course: “Recent Advances of High-level Synthesis”, ShanghaiTech University, July 2017.
- Week-long short course: “Digital Design with FPGAs”, Training course for engineers of Jump Trading, August 2017 and December 2017.
- Panelist: “The Future of AI”, SingularityU Warsaw Chapter Conference, 2017.
- Panelist: “AI Chip”, SV Connect Conference, 2017.
- Panelist: “Smart Hardware”, SWEDCS, 2017.
- Tutorial presenter: “Accelerating Deep Neural Networks on FPGAs”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018.
- Short course: “Machine Learning and Its FPGA Acceleration”, ShanghaiTech University, 2019.
- Panelist: “Where will the computer architecture go?”, COOL Chips 22, Japan, 2019.
- Panelist: “New EDA tools: Beyond traditional EDA and new chances for start-ups”, AI Chips Summit, Hong Kong, 2019.
- Panelist: “High-Level Synthesis 1974-2020: The Meteoric Rise of a Hot Topic?”, ACM/IEEE Design Automation Conference (DAC), 2020.
- Panelist: NSF Workshop on Machine Learning and Hardware, 2020.
- Panelist: NSF Workshop on Micro/Nano Circuits and Systems design: Challenges and Opportunities, 2020.
- Panelist: “What is next on source-to-source transformation?”, Workshop at FPGA’2022: Open-Source Source-to-Source Transformation for High-Level Synthesis (HLS), 2022.
- Panelist: “Big Project Application and Management”, ACSIC Symposium on Frontiers in Computing (SOFC), 2022.
- Panelist: “Future of FPGAs for Deep Learning”, Tutorial on Deep Learning-Optimized FPGA Architectures, co-located with IEEE/ACM International Symposium on Microarchitecture (MICRO), 2022.
- Panelist and session chair: “EDA for domain specific computing”, International Symposium on Physical Design, 2023.
- Tutorial presenter: “ScaleHLS-HIDA: From PyTorch/C++ to Highly-optimized HLS Accelerators”, ACM/SIGDA International Symposium on FPGA, 2024.

Research Proposal Review

- External proposal reviewer, Natural Sciences and Engineering Research Council of Canada, 2008, 2009, 2010, 2019, 2020
- External proposal reviewer, Israel Science Foundation, 2008
- External research proposal reviewer, Qatar National Research Fund, 2009, 2011, 2012, 2014
- External research proposal reviewer, Nanyan Technology University, Singapore, 2010
- External proposal reviewer, Intramural Discovery Grant Program, Vanderbilt University, 2013
- Proposal reviewer for U. S. Army Research Office, 2014
- NSF panelist, 2012, 2015, 2016, 2019, 2020, 2021, 2022

Journal Paper Review

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Advanced Packaging (TAP)
- ACM Transactions on Reconfigurable Technology and Systems (TRETS)
- IEEE Transactions on Nanotechnology (TN)
- Integration, the VLSI Journal
- Journal of Low Power Electronics (JOLPE)
- IET Circuits, Devices & Systems
- IEEE Design & Test of Computers
- IEEE Transactions on Industrial Informatics
- Applied Physics A
- ACM Transactions on Architecture and Code Optimization (TACO)
- IEEE Transactions on Cyber-Physical Systems (TCPS)
- Briefings in Bioinformatics
- IEEE Transactions on Circuits and Systems for Video Technology
- BMC Bioinformatics
- IEEE Security and Privacy
- Nature Electronics

University Services

- Director, AMD/Xilinx Center of Excellence, 2020-present
- Thrust Co-lead, Hybrid Cloud Thrust, IBM-Illinois Discovery Accelerator Institute, 2021-present
- Elected into the Senate of University of Illinois, 2022-present
- Chief Scientist, IBM-Illinois Center for Cognitive Computing Systems Research, 2020-2021
- ECE Named Appointments Committee, 2022-present
- Chair, ECE Graduate Committee, 2020-2022
- ECE Promotion and Tenure Committee, 2016-present
- Steering Committee member, C-NICE center, Grainger College of Engineering, 2019-present
- Invited reviewer for Smart Transportation Infrastructure Initiative for the college, 2021
- Invited reviewer for proposals for Grainger College of Engineering (Small Equipment Grants, Sloan Call for Ideas, etc.), 2019-2020
- Search Committee member, Clinical or Teaching Faculty for ILEE (Innovation, Leadership, and Engineering Entrepreneurship), 2020

- University Delegation member visiting Foxconn Interconnect Technology (with Chancellor, Provost, and Dean), Taiwan, 2019
- University Delegation member meeting the CRRC Corporation Limited (with Provost and Dean), China, 2018
- Elected into the Senate of University of Illinois, 2018-2019
- Elected into the Executive Committee of Grainger College of Engineering, 2016-2019
- Invited reviewer for proposals for CoE's SRI Program, 2018
- Area Chair, Computer Engineering, 2015-2017
- Elected into the Senate of University of Illinois, 2013-2016
- Panelist, campus review panel for GYSS travel grant competition, 2015
- Alternate representative of CSL on the College Executive Committee, 2015-2016
- CSL Director Search Committee, 2014
- Chair, CE Lecturer Search Committee, 2014
- Member, EE Lecturer Search Committee, 2014
- ECE Curriculum Committee, 2013-2014
- CSL Policy and Planning Committee, 2008-2009, 2011-2012, 2014-2016, 2020-2021
- Computer Engineering Committee, 2008-2023
- Member of Teaching Evaluation and Awards Committee, 2005-2007
- Graduate ECE Seminar Committee, 2006-2007, 2009
- Graduate Committee, 2007-2009, 2011-2012
- Fellowship Committee, 2009-2012
- Colloquium Committee, 2010-2014
- CSL Build-out Committee, 2012
- Ph.D. committees (prelim exam and final defense):
  2006: Dr. Smruti Sarangi (CS, UIUC), Dr. Lei Cheng (CS, UIUC)
  2007: Dr. Liang Deng (ECE, UIUC), Dr. Yu Zhong (ECE, UIUC), Mr. Sain-Zee Ueng (ECE, UIUC), Dr. Yidnek Mekonnen (ECE, UIUC), Dr. Radu Teodorescu (CS, UIUC)
  2008: Dr. Zhiguo Qian (ECE, UIUC), Dr. Tomasz Czajkowski (ECE, U. of Toronto), Dr. Brian Greskamp (CS, UIUC), Dr. Rodolfo Pellizoni (CS, UIUC)
  2009: Dr. Chen Dong (ECE, UIUC)
  2010: Dr. Hui Kong (ECE, UIUC), Dr. Tan Yan (ECE, UIUC), Dr. John Kelm (ECE, UIUC), Dr. Lijuan Luo (ECE, UIUC), Dr. Lu Wan (ECE, UIUC), Dr. Yingying Kuai (ECE, UIUC)
  2011: Dr. Alex Papakonstantinou (ECE, UIUC), Dr. Joon Hyung Chung (ECE, UIUC), Dr. Neal Crago (ECE, UIUC), Dr. Hongbo Zhang (ECE, UIUC)
  2012: Dr. Qiang Ma (ECE, UIUC), Dr. John Stratton (ECE, UIUC), Dr. Xiao-Long Wu (ECE, UIUC), Dr. Feng Xiong (ECE, UIUC)
  2013: Dr. Yuelin Du (ECE, UIUC), Dr. Ting Yu (ECE, UIUC), Dr. Soobae Kim (ECE, UIUC)
  2014: Dr. Eric Kim (ECE, UIUC),
  2015: Dr. Rajesh Bhana (ECE, UIUC), Dr. Yun Heo (ECE, UIUC), Dr. Hee-Seok Kim (ECE, UIUC), Dr. Christine Ying-Yu Chen (ECE, UIUC), Dr. Jungwook Choi (ECE, UIUC), Dr. Pei-Ci Wu (ECE, UIUC), Dr. Kuo-Hsuan Meng (ECE, UIUC), Dr. Joe Meng (ECE, UIUC).
  2016: Dr. Maryam Kazerooni (ECE, UIUC), Dr. Haitong Tian (ECE, UIUC), Dr. Jongsok Choi (External Examiner, ECE, U. of Toronto).
  2017: Dr. Choden Konigsmark (ECE, UIUC), Dr. Siming Guo (ECE, UIUC), Dr. Wonhyeok Jang (ECE, UIUC), Dr. Tsung-Wei Huang (ECE, UIUC), Dr. Henry Duwe (ECE, UIUC), Dr. Romesh Nandwana (ECE, UIUC), Dr. Nicholas Thomson (ECE, UIUC), Dr. Keith Campbell (ECE, UIUC), Dr. Glenn Ko (CS, UIUC), Dr. Chen-Hsuan Lin (ECE,

UIUC), Dr. Ti Xu (ECE, UIUC), Dr. Guanwen Zhong (External Examiner, CS, National U of Singapore), Dr. Hao Liang (External Examiner, ECE, Hong Kong U of Science and Technology).

2018: Dr. Johnathan Alsop (ECE, UIUC), Dr. Izzat El Hajj (ECE, UIUC), Dr. Leslie Hwang (ECE, UIUC).

2019: Dr. Di He (ECE, UIUC), Dr. Yi Liang (ECE, UIUC), Dr. Daifeng Guo (ECE, UIUC).

2020: Dr. Tianqi Gao (ECE, UIUC), Dr. Chun Xun Lin (ECE, UIUC), Dr. Xinying Wang (ECE, UIUC).

2021: Dr. Ashutosh Dhar (ECE, UIUC), Dr. Sitao Huang (ECE, UIUC), Dr. Xinheng Liu (ECE, UIUC), Dr. Azin Heidarshenas (CS, UIUC).

2022: Dr. Adel Ejjeh (CS, UIUC), Dr. Seung Won Min (ECE, UIUC), Dr. Mohammad AlMasri (ECE, UIUC), Dr. Yifan Yuan (ECE, UIUC), Dr. Iou-Jen Liu (ECE, UIUC), Dr. Xiaofan Zhang (ECE, UIUC), Dr. Vikram Sharma Mailthody (ECE, UIUC), Dr. Youjie Li (ECE, UIUC), Dr. Zijing Zhao (ECE, UIUC).

2023: Dr. Guannan Guo (ECE, UIUC), Dr. Tin-Yin Lai (ECE, UIUC), Dr. Wei Zuo (ECE, UIUC), Dr. Anand Ramachandran (ECE, UIUC), Mr. Kun Wu (ECE, UIUC), Mr. Yuhong Li (ECE, UIUC), Mr. Hanchen Ye (ECE, UIUC), Mr. Junhao Pan (ECE, UIUC).

2024: Ms. Qian Jiang (ECE, UIUC)

Invited Talks

Title	Conference or Seminar	Location	Year
1. Design and Synthesis for Low-Power FPGAs	Seminar	Altera Corp., San Jose	2005
2. VLSI design: turning your big ideas into reality	ECE 200: Undergraduate Seminar	UIUC	2006
3. Technology Mapping Algorithms for Programmable Logic Devices	ECE 500: Graduate Seminar	UIUC	2006
4. Abstraction beyond RTL for Low-Power	Computer Engineering Seminar	UIUC	2006
5. Design and Synthesis for Low-Power FPGAs	Seminar	Velogix Inc., San Jose	2006
6. 3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA Architecture	ECE 590B: Electromagnetics, Optics & Remote Sensing Seminar	UIUC	2007
7. System, Behavioral, and Logic Level Design Automation	Seminar	T.J. Watson Research Center, IBM, USA	2007
8. 3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA Architecture	Computer Engineering/Circuits Seminar	UIUC	2007
9. 3D nFPGA: A CMOS/Nanomaterial Hybrid Reconfigurable Architecture	Workshop on SoC Design Methodologies	Seoul National University, Seoul, Korea	2007
10. Design and Synthesis for Low-Power FPGAs	Seminar	Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China	2007
11. VEBoC: Variation and Error-Aware Design for Billions of Devices on a Chip	IEEE/ACM Asia and South Pacific Design Automation Conference	Seoul, Korea	2008
12. New Design Techniques and Architectures for FPGAs	ECE Seminar	University of Toronto, Toronto, Canada	2008

13. New Design Techniques and Architectures for FPGAs	Seminar	Altera Corp., Toronto	2008
14. New Design Techniques and Architectures for FPGAs	Seminar	Xilinx Corp., Toronto	2008
15. EPOS: an Explicitly Parallel Operations System	Workshop of SoC Design Methodologies	National Tsing Hua University, Taiwan	2008
16. New Synthesis and Architecture Solutions for Reconfigurable ICs	DLP and VLSI/CAD Workshop	National Tsing Hua University, Taiwan	2008
17. New Synthesis and Architecture Solutions for Reconfigurable ICs	EE Seminar	National Taiwan University, Taiwan	2008
18. Variation-Aware Chip Design for Reliability and Performance	Seminar	Sun Microsystems, Inc., USA	2008
19. Reconfigurable Circuits Design with Nanomaterials	Design, Automation and Test in Europe (DATE)	Nice, France	2009
20. New Binding Algorithms for Glitch and Inter-transition Power Reduction	ECSI and USB Workshop on High Level Synthesis: Next Step to Efficient ESL Design	Yokohama, Japan	2009
21. Nano 3D FPGAs: Design and CAD	Seminar	T.J. Watson Research Center, IBM, USA	2009
22. FPCNA: A Field Programmable Carbon Nanotube Array	Global COE Workshop	Wasada University, Japan	2009
23. Design and CAD for Nanoscale Reconfigurable Logic	EE Seminar	Stanford University	2009
24. New Design Techniques for Existing and Futuristic FPGAs	EECS Seminar	UC Berkeley	2009
25. Reconfigurable Computing for High Performance	CS Seminar	National University of Singapore	2010
26. Reconfigurable Computing for High Performance	CE Seminar	Nanyang Technological University, Singapore	2010
27. New Design Techniques for Existing and Futuristic FPGAs	CSSI Seminar	Carnegie Mellon University	2010
28. Challenges and Opportunities of ESL Design Automation	Electronic Design Processes Symposium	Monterey, CA	2010
29. Compilation and Optimization for High Performance	ECE Seminar	Purdue University	2010
30. FCUDA: Enabling Efficient Compilation of CUDA Kernels onto FPGAs	Asia South Pacific Design Automation Workshop	Incheon, Korea	2010
31. Challenges and Opportunities of ESL Design Automation	Electronic Design Processes Symposium	Monterey, CA	2010
32. FCUDA: Efficient CUDA Kernel Compilation for High-Performance Computing on FPGAs	Seminar	NEC, Tokyo, Japan	2011
33. 3D FPGAs with Nanotechnology	NYU-AD 3D Workshop	Abu Dhabi, United Arab Emirates	2011
34. Porting Performance across GPUs and FPGAs	Pre-conference Workshop at FCCM	Salt Lake City, Utah	2011
35. Porting Performance across GPUs and FPGAs through Multilevel Granularity	eSeminar	GSRC (Gigascale Systems Research Center), USA	2011

Parallelism			
36. Design and CAD for 3D Reconfigurable Circuits	Symposium on 3D TSV Processes and Design Challenges	Singapore	2011
37. FCUDA: Porting Performance across GPUs and FPGAs	Web seminar	Intel, Oregon	2011
38. High Level Synthesis of FPGA and Future Nanoscale FPGA Design	Graduate Seminar, School of Information Science and Technology, Xiamen University	Xiamen, China	2011
39. Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	PIC Seminar, IBM	T.J. Watson Research Center, Yorktown Heights	2011
40. 3D FPGAs with Nanotechnology	Nanoelectronic Devices for Defense & Security Conference	New York	2011
41. High-level Synthesis for FPGA and Futuristic 3D FPGA Design	Departmental Seminar	National Taiwan University	2011
42. High-level Synthesis for FPGA and Futuristic 3D FPGA Design	Departmental Seminar	National Tsing Hua University, Taiwan	2011
43. Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	Departmental Seminar	University of Wisconsin at Madison	2012
44. Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	Departmental Seminar	University of Illinois at Chicago	2012
45. Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	AMD Research Center, Beijing	2012
46. Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	Tsinghua University, China	2012
47. Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	Microsoft Research Center, Beijing	2012
48. Control Flow Optimization for GPU Computing and Other Research Highlights	Special CS Seminar	Stanford University	2012
49. GPU Computing and the CUDA-to-FPGA Compiler	Departmental Seminar	University of California at Riverside	2012
50. GPU Computing and the CUDA-to-FPGA Compiler	Invited panel presentation	T.J. Watson Research Center, Yorktown Heights	2013
51. GPU Computing and the CUDA-to-FPGA Compiler	Departmental Seminar	Imperial College, London	2013
52. Optimizations in GPU: Smart Compilers and Core-level	ACM/IEEE System Level Interconnect Prediction	Austin, TX	2013

Reconfiguration			
53. Is Graphene Useful for Digital Circuits?	EDA Workshop	Kyoto, Japan	2013
54. Graphene Nano-Ribbon Field-Effect Transistors as Future Low-Power Devices	IEEE/ACM International Symposium on Low Power Electronics and Design	Beijing, China	2013
55. Compiler Optimization for GPU Computing	Departmental Seminar	National Taiwan University, Taiwan	2014
56. Compiler Optimization for GPU Computing	Special Seminar	National Chiao Tung University, Taiwan	2014
57. New Solutions for High-level Synthesis	Special Seminar	University of Southern California	2014
58. New Solutions for System and High-level Synthesis	Special Seminar	Harvard University	2014
59. New Solutions for High Level Synthesis	eSeminar	C-FAR Research Center	2014
60. New Solutions for System and High-level Synthesis	CS Seminar	School of Computing, National University of Singapore	2014
61. New Algorithms for Computation Acceleration for Large-scale Smart Grids	IEEE International Conference on Solid-State and Integrated Circuit Technology	Guilin, China	2014
62. FCUDA: the CUDA to FPGA Compiler	ICCAD 2014 Workshop: Heterogeneous Computing Platforms (HCP)	San Jose, CA	2014
63. New Solutions for System-Level and High-Level Synthesis	IEEE International Symposium on Integrated Circuits	Singapore	2014
64. Reliability, Security, and Design Productivity in the Era of IoT	IEEE International Conference on Anti-counterfeiting, Security, and Identification	Macau, China	2014
65. Boosting Design Productivity for the Internet of Billons of Things	Advanced Digital Sciences Center	Singapore	2014
66. Quantifying and Improving the Accuracy of Detecting Genomic Variation	NSF I/UCRC Planning Workshop	Chicago, IL	2015
67. Boosting Design Productivity for the Internet of Billons of Things	China Semiconductor Technology International Conference (CSTIC)	Shanghai, China	2015
68. Improving Design Productivity for High-Performance and Energy-Efficient Circuits	Special Seminar	Qualcomm, San Jose	2015
69. New High-level Synthesis Techniques for High-Performance, Energy-Efficiency, and Reliability	Special Seminar	University of Bologna, Bologna, Italy	2015
70. High Design Productivity for Reliable and Energy-Efficient Circuits in the Era	Special Seminar	Fudan University, China	2015

of Internet of Things			
71. High-Level Synthesis, Computational Genomics and Emerging Technologies	Invited talk in a panel	Zhejiang University, China	2015
72. High Design Productivity for Reliable and Energy-Efficient Circuits in the Era of Internet of Things	IEEE International Conference on ASIC	Chengdu, China	2015
73. Designing High-Quality Hardware on a Development Effort Budget: A Study of the Current State of High-Level Synthesis	IEEE/ACM Asia and South Pacific Design Automation Conference	Macau, China	2016
74. System Design Automation Techniques for FPGAs with High-Performance, Energy-Efficiency, and Reliability	Special Seminar	Toyota, San Jose	2016
75. Reliable and Energy-Efficient Circuit Design in the Era of Internet of Things	Departmental Seminar	Peking University, China	2016
76. New Advances on High-Level Synthesis	Departmental Seminar	Tsinghua University, China	2016
77. The CUDA to FPGA Compiler	ShanghaiTech Workshop on Emerging Devices, Circuits and Systems	Shanghai, China	2016
78. SoC, NoC and Hierarchical Bus Implementations of Applications on FPGAs Using the FCUDA Flow	IEEE Computer Society Annual Symposium on VLSI	Pittsburgh, USA	2016
79. System Design Automation Techniques for FPGAs with High-Performance, Energy-Efficiency, and Reliability	Special Seminar	Huawei, China	2016
80. The CUDA to FPGA Compiler	Workshop on FPGAs for Scientific Simulation and Data Analytics	University of Illinois, USA	2016
81. Automated System-Level Co-design: Are We Finally Ready?	Future Chip 2016: Challenges and Opportunities of Design Automation in China	Tsinghua University, China	2016
82. Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	National Taiwan University, Taiwan	2017
83. Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	National Tsing Hua University, Taiwan	2017
84. Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	National Cheng Kung University, Taiwan	2017
85. Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Special Seminar	Microsoft Research Lab, Seattle, USA	2017
86. Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	ShanghaiTech Workshop on Emerging Devices, Circuits and Systems (SWEDCS'2017)	ShanghaiTech University, China	2017
87. Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	ICC Distinguished Lecture	Michigan Technological University, Michigan	2017

88. Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	Workshop on Challenges and Opportunities of AI Chips	Tsinghua University, China	2017
89. FPGA-based Smart Devices and Platforms for the AI Revolution	SingularityU Warsaw Chapter Conference and Masters & Robots Conference	Warsaw, Poland	2017
90. Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	Special Seminar	Bitmain Inc., China	2017
91. Hardware-Software Co-design and Heterogeneous Computing in the IoT Era	Huawei-Illinois Workshop	Champaign, IL	2017
92. Machine Learning on FPGAs to Face the IoT Revolution	International Conference on Computer-Aided Design (ICCAD'17)	Irvine, CA	2017
93. Machine Learning on FPGAs to Face the IoT Revolution	Future Chips 2017 – Smart Chips, Smart World	Tsinghua U, Beijing	2017
94. AI Chip for Smart Sound	SV Connect Conference	Santa Clara, CA	2018
95. Deep Learning for Better Variant Calling for Cancer Diagnosis and Treatment	ASPDAC'18	Jeju Island, Korea	2018
96. New Algorithms and Hardware Acceleration for the IoT Revolution	Special Seminar	Stanford University, CA	2018
97. New Algorithms and Hardware Acceleration for the IoT Revolution	ChinaDA 2018 Conference	Peking University, China	2018
98. New Algorithms and Hardware Acceleration for the IoT Revolution	Special Seminar	Beihang University, China	2018
99. New Algorithms and Hardware Acceleration for the IoT Revolution	Departmental Seminar	Southeast University, China	2018
100. New Algorithms and Hardware Acceleration for the IoT Revolution	Special Seminar	Anlogic, Inc., China	2018
101. Cognitive Computing on Large FPGA Networks	Workshop on ZJU-UIUC joint collaboration	International Campus, Zhejiang University, China	2018
102. Overcoming Challenges of Accelerating Deep Neural Network Computations	Plenary Talk	IEEE Computer Society Annual Symposium on VLSI, Hong Kong	2018
103. Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	HC Torng Lecture	Cornell University	2018

104. Design Productivity, Compilation, and Acceleration for Data Analytic Applications	Keynote Speech	International Conference on Big Data Analytics & Data Mining, Chicago	2018
105. Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Special Seminar	Beijing Institute of Technology, China	2018
106. Design Productivity, Compilation, and Acceleration for Data Analytic Tasks in Structural Health Monitoring	CRRC HSM Symposium	Qingdao, China	2018
107. Reconfigurable Software and Hardware – A New Paradigm	Future Chips, 2018	Tsinghua University, China	2018
108. DNNBuilder: an Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs	e-Seminar	Xilinx, Inc., USA	2018
109. Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Special Seminar	Yitu, Inc., Singapore	2019
110. Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Special Session Distinguished Talk, COOL Chips	Yokohama, Japan	2019
111. Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Keynote speech	Computing Conference, London, England	2019
112. Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Special Seminar	Umbo Computer Vision, Inc., Taipei, Taiwan	2019
113. A Hybrid GPU + FPGA System Design for Autonomous Driving Cars	Invited talk	IEEE Intl. Workshop on Signal Processing Systems, China	2019
114. Cognitive Computing on Heterogeneous Hardware Systems for the AI Revolution	Keynote speech	The IEEE International Workshop on Signal Processing Systems, China	2019
115. Design for Smart IoT Devices	Invited Talk	Annual World Congress of Nano Science & Technology, China	2019
116. Design, Compilation, and Acceleration for Deep Neural Networks in IoT Applications	Distinguished Seminar Series, Honor Society of School of Information Science and Engineering	Southeast University, China	2019
117. Computing with Heterogeneous Hardware Systems for the AI Revolution	Keynote speech	AI Chips Summit, Hong Kong, China	2019
118. New Trend on High-Level Synthesis and Customized Compiler for Edge Intelligence	Designers' Forum	IEEE/ACM Asia and South Pacific Design Automation Conference, Beijing, China	2020

119. SkyNet: A Champion DNN Model for Low Power Object Detection	Invited Talk	ACM Workshop on Simplifying Edge and Mobile Intelligence	2020
120. Cognitive Computing on Heterogenous Hardware Systems for the AI Revolution	Distinguished Speaker Series	ACM Sacramento Chapter	2020
121. Elegant and Effective Co-design of Machine-Learning Algorithms and Hardware Accelerators	Keynote speech	Workshop on ROAD4NN: Research Open Automatic Design for Neural Networks	2020
122. Effective Algorithm-Accelerator Co-design for AI Solutions on Edge Devices	Keynote speech	ACM Great Lakes Symposium on VLSI	2020
123. Effective Co-design of Deep Learning Algorithms and Hardware Accelerators	Invited talk	2nd Workshop on Accelerator Computer Aided Design	2020
124. VecQ: Minimal Loss DNN Model Compression with Vectorized Weight Quantization	Invited talk	Workshop on Hardware and Algorithms for Learning On-a-chip	2020
125. Elegant and Effective Co-design of ML Algorithms and Accelerator	Invited Talk	Rice University ECE Distinguished Speaker Series	2020
126. Advanced Co-design of Deep Learning Algorithms and Hardware Accelerators	Keynote Speech	IEEE Intl. Conf. on Field-Programmable Technology	2020
127. New Machine Learning and Hardware Accelerator Designs for Security	Invited Talk	Workshop on Cybersecurity for OT Systems, Singapore	2021
128. Deep Learning Algorithms and Hardware Co-Design for Edge Computing	Departmental Seminar	ECE, Texas A&M Univ.	2021
129. UIUC Xilinx Adaptive Compute Cluster (XACC)	Invited Talk	Xilinx Adaptive Compute Cluster Summit	2021
130. Design of Reconfigurable Computing Systems for Smart IoT Applications	Keynote Speech	Workshop on Reconfigurable Computing for Machine Learning – RC4ML	2021
131. Design of Reconfigurable Computing Systems for Smart IoT Applications	ACM Distinguished Speaker Series	Universidad Católica San Pablo, Peru	2021
132. Fast and Generic Neural Architecture Search via Regression	Rutgers ECE Colloquium	Rutgers, The State University of New Jersey	2021
133. Fast and Generic Neural Architecture Search via Regression	ECE Grad Seminar	University of Pittsburgh	2021
134. AccGuard: Secure and Trusted Computation on Remote FPGA Accelerators	Invited Talk	RSS2: Workshop on Robustness and Safe Software 2.0, co-located	2022

		with ASPLOS'22	
135. AI Algorithm and Accelerator Co-design for Computing on the Edge	Invited talk	IEEE International Workshop on Electronic Design Automation and Machine Learning (EDAML)	2022
136. Design of Reconfigurable Computing Systems for Accelerating Smart IoT Applications	APUP Speaker Series	Synopsys	2022
137. ScaleHLS: A Scalable High-Level Synthesis Framework with Multi-level Transformations and Optimizations	Invited talk	ACM/IEEE Design Automation Conference	2022
138. ScaleHLS: A Scalable High-Level Synthesis Framework with Multi-level Transformations and Optimizations	Invited talk	Stanford Univ	2022
139. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	CS Colloquium	Princeton Univ	2022
140. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	Distinguished Lecture	Northwestern Univ	2022
141. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	Departmental Seminar	Lehigh Univ	2022
142. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	Invited talk	UCLA	2022
143. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	Departmental Seminar	UCSD	2022
144. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	Departmental Seminar	UCI	2022
145. FPGA Virtualization and Compilation for Serverless Computing	Invited Lecture	Princeton Univ	2023
146. IoT and AI Revolution	Invited Lecture	Women in ECE, student organization, UIUC	2023
147. Lightning Talk: The Next Wave of High-level Synthesis	Invited Talk	IEEE/ACM Design Automation Conf	2023
148. Programmability, Scalability, and Security for Heterogenous Computing with FPGAs	Invited Talk	IEEE/ACM Design Automation Conf	2023
149. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	College of EECS Seminar	National Taiwan University	2023
150. Programmability, Scalability, and Security for Reconfigurable Computing in the Cloud	CS Departmental Seminar	National University of Singapore	2023
151. Design, Compilation, and Acceleration for Deep Neural Networks	Special Seminar	Temasek Polytechnic, Singapore	2023

in IoT Applications			
152. ScaleHLS: a Fully Automated PyTorch-to-Hardware Design Flow	Departmental Seminar	University of South Florida	2023
153. Software/Hardware Co-design for LLM and Its Application for Design Verification	Invited Talk in a Special Session	IEEE/ACM Asia and South Pacific Design Automation Conference, South Korea	2024

News Articles or Announcements

Grainger Engineering Joins New AI Alliance to Enhance Open Source Technology
https://grainger.dev.engr.illinois.edu/news/stories/60868

Looking up: scaling up high-level synthesis for faster, more efficient chip design
https://ece.illinois.edu/newsroom/news/59100

IBM-Illinois connection spurs on collaborative learning, research opportunities
https://grainger.illinois.edu/news/stories/58732?utm_source=ECE+news&utm_medium=website&utm_id=ECE+news

How Illinois and IBM want to combine the best of both worlds for an "ideal" hybrid cloud
https://grainger.illinois.edu/news/i2cloud

Students spent the summer at IBM in unusual new externship program
https://discoveryacceleratorinstitute.grainger.illinois.edu/newsroom/52266

University of Illinois researchers are part of a $15M institute developing real-time artificial intelligence to accelerate discovery in data-driven science
https://ece.illinois.edu/newsroom/news/42827

New tool improves accuracy, customization in DNA sequencing capabilities
https://csl.illinois.edu/news/42444

Sitao Huang Joined UC Irvine as an Assistant Professor
https://engineering.uci.edu/users/sitao-huang

Cong (Callie) Hao Joined GeorgiaTech as an Assistant Professor
https://callie.ece.gatech.edu

CSL Student Receives 2020 Google Ph.D. Fellowship
https://csl.illinois.edu/news/csl-student-receives-2020-google-phd-fellowship

Chen and Hwu lead Illinois in establishing advanced research cluster with Xilinx
https://ece.illinois.edu/newsroom/news/9233

Illinois Named Xilinx Center of Excellence
https://csl.illinois.edu/news/illinois-named-xilinx-center-excellence

Best Paper Award from VLSID'20
https://www.c3sr.com/post/2020/20200104_vlsidaward/

Double Championships at DAC System Design Contest 2019
https://www.c3sr.com/post/2019/20190605_sdcawards/

Chen's Inspirit IoT Listed Among 10 Hottest Industrial IoT Startups
https://ece.illinois.edu/newsroom/article/30579

Chen Named as Next Editor-in-Chief of ACM TRETS
https://ece.illinois.edu/newsroom/article/29157

Chen and Choudhury Elevated as IEEE Fellows
https://ece.illinois.edu/newsroom/article/29123

ICCAD Best Paper Award, 2018
http://dchen.ece.illinois.edu/ICCAD18.html

Chen's Inspirit IoT Startup Awarded Phase II NSF SBIR Grant
https://www.prnewswire.com/news-releases/inspirit-iot-awarded-phase-ii-nsf-sbir-grant-to-support-development-of-dnn-architect-300720038.html

ECE Illinois Researchers Pursue World Class Computing and Programmability Through DARDA Project
https://ece.illinois.edu/newsroom/article/27542

Chen's Inspirit IoT Startup Making Waves in Industry, Academia
https://csl.illinois.edu/news/chen%E2%80%99s-inspirit-iot-startup-making-waves-industry-academia

Wired In: Deming Chen | News-Gazette.com
http://www.news-gazette.com/news/business/2017-09-17/wired-deming-chen.html

LOW-COST AUDIO SECURITY SYSTEM HELPS RESEARCHERS WIN IEEE COMPETITION
https://ece.illinois.edu/newsroom/article/23447

Illinois, start-up researchers win DAC-IoT competition with low-cost audio security system
https://csl.illinois.edu/news/illinois-start-researchers-win-dac-iot-competition-low-cost-audio-security-system

ICCAD Best Paper Award, 2015
https://www.ece.illinois.edu/newsroom/article/15131

Chen and Li Named 2015 Willett Scholars
http://www.ece.illinois.edu/newsroom/article/11139

Faculty receive IBM recognition, funding for research contributions
http://csl.illinois.edu/news/faculty-receive-ibm-recognition-funding-research-contributions

Researchers Release First SPICE-compatible Compact Models for Graphene-based Digital Circuits
http://csl.illinois.edu/news/researchers-release-first-spice-compatible-compact-models-graphene-based-digital-circuits

High-level Synthesis on Fire: Research Receives Recognition from Academia, Industry
http://www.ece.illinois.edu/mediacenter/article.asp?id=6013

ECE Receives Zedboard Donation for Research, Education
http://www.ece.illinois.edu/mediacenter/article.asp?id=7389

Chen Receives Intel Gift to Study Increasing Computer Performance and Efficiency
http://www.ece.illinois.edu/mediacenter/article.asp?id=1686

ECE Faculty and Students Win IEEE FCCM Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=1270

Chen and Hwu Win IEEE SASP'09 Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=512

Chen Promotes Nanotechnology Research
http://www.ece.illinois.edu/mediacenter/article.asp?id=182

Graduate Students and Professor Team Up to Win Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=181

ECE Faculty Receive CAREER Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=176

Illinois Named an OpenSPARC Center of Excellence
http://www.ece.illinois.edu/mediacenter/article.asp?id=366

Open-Source Tool Releases (incomplete list)

- **GNRFET HSPICE Model**: First parameterized HSPICE transistor compact models of two types of Graphene Nano-Ribbon Field-Effect Transistors, MOS-GNRFET and SB-GNRFET. Available at nanoHUB.org since July 2013. (>2000 downloads.)

  Download: http://dchen.ece.illinois.edu/tools.html

- **BLESS**: Bloom-filter-based Error Correction Solution for High throughput Sequencing Reads. Currently, the best DNA error correction tool in terms of quality and small memory usage. Available since January 2014. (>3000 downloads.)

  Download: http://dchen.ece.illinois.edu/tools.html

- **TIGER**: Tiled Iterative Genome Assembler. Significant improvement over state-of-the-art *de novo* genome assemblers. Available since 2013.

  Download: http://impact.crhc.illinois.edu/Tiger/tiger.aspx

- **H.264 HLS Benchmark**: Fully synthesizable H.264 Video Decoder code, which can be synthesized into RTL with high-level synthesis for FPGA implementation and achieve real-time decoding. Available since 2016.

  Download: http://dchen.ece.illinois.edu/tools.html

- **TMDFET SPICE Model**: SPICE transistor models of flexible Transition Metal Dichalcogenide Field-Effect Transistors, TMDFET. Available at nanoHUB.org since 2016. (>600 downloads.)

Download: http://dchen.ece.illinois.edu/tools.html

- **FCUDA**: A system-synthesis compiler to map GPU CUDA code to FPGA. Enable a common frontend language for heterogeneous compute platforms where FPGA and GPU co-exist. Low-power FPGA computing with comparable performance as GPU. FCUDA project has produced two Best Paper Awards for the conferences SASP'09 and FCCM'11. Available since 2016.

  Download: http://dchen.ece.illinois.edu/tools.html

- **RIP**: This open-source project contains three inter-related software packages (fast software modeling, fast hardware modeling and design space exploration (DSE), and hardware/software co-design), for the ultimate task of automated hardware/software partitioning targeting either sophisticated SoC designs or computing on heterogeneous systems. The paper for fast hardware modeling and DSE embedded in this package has won the IEEE/ACM William J. McCalla ICCAD Best Paper Award in 2015. Available since 2017.

  Download: https://github.com/UIUC-ChenLab/rip

- **Cloud-DNN**: Cloud-DNN is an open-source framework that maps DNN (deep neural network) models trained by Caffe to FPGAs in the cloud for inference acceleration. It takes the input *.prototxt DNN description, generates corresponding C++ network description, and then produces the final hardware accelerator IPs through high-level synthesis. The goal of Cloud-DNN is to provide more flexible and user-friendly DNN acceleration on cloud-FPGAs (e.g., AWS F1). Available since 2019.

  Download: https://github.com/microideax/Open-Dnn

- **DNNBuilder**: This package provides a novel solution that can automatically convert the Caffe trained DNN to the FPGA RTL level implementation without involving any hardware programming effort. It also provides uniform APIs to the users for their AI recognition task. The developers, without any FPGA programming experience, can deploy their FPGA accelerated deep learning services for both cloud and edge computing, only by providing their trained Caffe models. The paper for DNNBuilder has won the *IEEE/ACM William J. McCalla ICCAD Best Paper Award* in 2018. Available since 2019.

  Download: https://github.com/IBM/AccDNN

- **T-DLA**: T-DLA (Ternarized Deep Learning Accelerator) is an open-source microprocessor designed specifically for accelerating DNN models trained with ternarized weights. This is the first instruction-based DLA design targeting ternary-quantized weights. T-DLA can deliver up to 0.4TOPS with 2.576W power consumption, showing 873.6× and 5.1× higher performance (fps/W) on ImageNet with Resnet-18 model comparing to Xeon E5-2630 CPU and Nvidia 1080 Ti GPU. Available since 2019.

  Download: https://github.com/microideax/T-DLA

- **DNN IPs**: This IP Package includes an open-source IP repository specifically designed for machine learning applications. The IPs include: Standard convolution IPs, Depth-wise separable convolution IPs, Pooling IPs, Bounding box regression IP, and Long-term Recurrent Convolutional Network IP. Each IP is provided with: introduction, interface description, inputs and outputs description, parameter configuration, and resource and performance. The IPs are developed in C/C++. The source code is synthesizable and RTL code can be generated conveniently using Xilinx Vivado HLS. Available since 2019.

  Download: https://github.com/DNN-Accelerators/Open-Source-IPs

- **Thanos:** This open-source package introduces Thanos, a fast graph partitioning tool which uses the cross-decomposition algorithm that iteratively partitions a graph. It also produces balanced loads of partitions. The algorithm is well suited for parallel GPU programming which leads to fast and high-

quality graph partitioning solutions. Experimental results show that we have achieved a 30x speedup and 35% better edge cut reduction compared to the CPU version of the popular graph partitioning tool METIS on average. Available since 2019.

Download: https://github.com/dannyk0104/thanos

- **µL2Q:** This open-source package introduces an ultra-low loss quantization (µL2Q) method that provides DNN quantization schemes based on comprehensive quantitative data analysis. µL2Q builds the transformation of the original data to a data space with standard normal distribution, and then finds the optimal parameters to minimize the loss of the quantization of a target bitwidth. Our method can deliver consistent accuracy improvements compared to the state-of-the-art quantization solutions with the same compression ratio. Available since 2019.

  Download: https://github.com/microideax/Quantization-caffe

- **SkyNet:** SkyNet is a new hardware-efficient DNN model specialized in object detection and tracking. SkyNet was developed based on the *SkyNet Design Methodology* to facilitate edge AI solutions, and demonstrated in the *56th IEEE/ACM Design Automation Conference System Design Contest (DAC-SDC)*, a low power object detection challenge for real-life unmanned aerial vehicle (UAV) applications. SkyNet won the *First Place Award* for both GPU and FPGA tracks of the contest in 2019. Available since 2019.

  Download: https://github.com/TomG008/SkyNet

- **AutoDNNchip:** AutoDNNchip is a design flow able to target different accelerator platforms such as FPGA, TPU, GPU, and ASIC. AutoDNNchip can produce either FPGA-based AI accelerators or ASIC AI chip designs and achieve better (up to 3.86× improvement) performance over expert-crafted state-of-the-art AI chip solutions. This provides a valuable framework for producing and evaluating different types of hardware accelerators to find the best or the most suitable ones that can be deployed to various AI applications. Available since 2020.

  Download: https://github.com/RICE-EIC/AutoDNNchip

- **FracBNN:** FracBNN is a binary neural network, which achieves MobileNetV2-level accuracy by leveraging fractional activations. In the meantime, its input layer is binarized using a novel thermometer encoding with minimal accuracy degradation, which improves the hardware resource efficiency. *The paper for FracBNN was a Best Paper Candidate at the ACM/SIGDA International Symposium on Field Programmable Gate Arrays* in 2021. Available since 2021.

  Download: https://github.com/cornell-zhang/FracBNN

- **ThunderGP:** ThunderGP enables data scientists to enjoy the *performance* of FPGA-based graph processing without compromising *programmability*. *To our best knowledge and experiments, this is the fastest graph processing framework on HLS-based FPGAs.* Available since 2021.

  Download: https://github.com/Xtra-Computing/ThunderGP

- **TwinDNN:** TwinDNN system pairs a high-accuracy heavy-duty network with a low-latency light-weight (e.g., highly compressed) network using a hierarchical inference logic that will infer high-accuracy network when the prediction of low-latency network is not considered confident. TwinDNN can recover up to 94% of accuracy drop caused by extreme network compression, with more than 90% speedup. Available since 2021.

  Download: https://github.com/jeonghm9764/TwinDNN

- **WinoCNN:** WinoCNN combines systolic array and fast Winograd algorithm for CNN acceleration. This system supports flexible convolution kernel sizes without sacrificing DSP efficiency through various algorithmic, architecture and on-chip memory subsystem designs and optimizations. Overall,

our accelerator delivers high throughput and state-of-the-art DSP efficiency compared to previous accelerator implementations. Available since 2021.

Download: https://github.com/xliu0709/WinoCNN

- **NEW! HELLO:** HELLO is a new DNA variant calling tool, where we use novel DNN (Deep Neural Network) architectures and customized variant inference functions that account for the underlying nature of sequencing data. Our method allows vastly smaller DNNs to outperform the Inception-v3 architecture used in DeepVariant for indel and substitution-type variant calls. Our improved accuracy and problem-specific customization of DNN models could enable more accurate pipelines and further method development in the field. Available since 2021.

  Download: https://github.com/anands-repo/hello

- **NEW! PyLog:** PyLog is a high-level, algorithm-centric Python-based programming and synthesis flow for FPGA. PyLog is powered by a set of compiler optimization passes and a type inference system to generate high-quality design. PyLog takes in Python functions, generates PyLog intermediate representation (PyLog IR), performs several optimization passes, including pragma insertion, design space exploration, and memory customization, etc., and creates the complete FPGA system design. PyLog also has a runtime that allows users to run the PyLog code directly on the target FPGA platform without any extra code development. Available since 2021.

  Download: https://github.com/hst10/pylog

- **NEW! ScaleHLS+HIDA:** ScaleHLS is a High-level Synthesis (HLS) framework on MLIR. ScaleHLS can compile HLS C/C++ or PyTorch model to optimized HLS C/C++ in order to generate high-efficiency RTL design using downstream tools, such as AMD Vitis HLS. By using the MLIR framework that can be better tuned to particular algorithms at different representation levels, ScaleHLS is more scalable and customizable towards various applications coming with intrinsic structural or functional hierarchies. Working with a set of neural networks modeled in PyTorch, ScaleHLS-generated hardware designs provide up to 3825x higher performances compared to the baseline designs that do not contain pragma directives and are only optimized by Xilinx Vivado HLS. Furthermore, HIDA (ScaleHLS 2.0) achieves an 8.54x higher throughput on average compared to that of ScaleHLS. Meanwhile, despite being fully automated and able to handle various applications, HIDA achieves a 1.29x higher throughput over DNNBuilder, a state-of-the-art RTL-based neural network accelerator on FPGAs.

  Available since 2022. **(>3000 downloads.)**

  Download: https://github.com/UIUC-ChenLab/ScaleHLS-HIDA

- **New! NimBlock:** This project focuses on enabling virtualization features to facilitate fine-grained FPGA sharing. We employ an overlay architecture which enables arbitrary, independent user logic to share portions of a single FPGA by dividing the FPGA into independently reconfigurable slots. We then explore scheduling possibilities to effectively time- and space-multiplex the virtualized FPGA. The Nimblock scheduling algorithm balances application priorities and performance degradation to improve response time and reduce deadline violations. We achieve up to 5.7× lower average response times when compared to a no-sharing and no-virtualization scheduling algorithm and up to 2.1× average response time improvement over competitive scheduling algorithms that support sharing within our virtualization environment.

  Available since 2023.

  Download: https://github.com/UIUC-ChenLab/Nimblock

- **New! FSLAM:** Simultaneous Localization and Mapping (SLAM) is one of the main components of autonomous navigation systems. With the increase in popularity of drones, autonomous navigation on

low-power systems is seeing widespread application. Most SLAM algorithms are computationally intensive and struggle to run in real-time on embedded devices with reasonable accuracy. We propose an FPGA-based SLAM system, named FSLAM, that accelerates the computationally intensive visual feature extraction and matching on hardware. FSLAM is based on a Zynq-family SoC and runs 8.5x, 1.55x and 1.35x faster compared to an ARM CPU, Intel Desktop CPU, and a state-of-the-art FPGA system respectively, while averaging a 2x improvement in accuracy compared to prior work on FPGA.

Available since 2023.

Download: https://github.com/vvemulapati/FSLAM

- **New! AccShield:** Machine learning accelerators such as the Tensor Processing Unit (TPU) are already being deployed in the hybrid cloud, and we foresee such accelerators proliferating in the future. In such scenarios, secure access to the acceleration service and trustworthiness of the underlying accelerators become a concern. In this work, we present AccShield, a new method to extend trusted execution environments (TEEs) to cloud accelerators which takes both isolation and multi-tenancy into security consideration. We demonstrate the feasibility of accelerator TEEs by a proof of concept on an FPGA board. Experiments with our prototype implementation also provide concrete results and insights for different design choices related to link encryption, isolation using partitioning and memory encryption, etc.

  Available since 2023.

  Download: https://github.com/UIUC-ChenLab/AccShield

- **NEW! PandoGen:** An ability to forecast future viral individuals at the sequence level enables advance preparation by characterizing the sequences and closing vulnerabilities in current preventative and therapeutic methods. In this work, we explore, in the context of a viral pandemic, the problem of generating complete instances of undiscovered viral protein sequences, which have a high likelihood of being discovered in the future using protein language models. Our novel method, called PandoGen, trains protein language models towards the pandemic protein forecasting task. PandoGen combines techniques such as synthetic data generation, conditional sequence generation, and reward-based learning, enabling the model to forecast future sequences, with a high propensity to spread. Applying our method to modeling the SARS-CoV-2 Spike protein sequence, we find empirically that our model forecasts twice as many novel sequences with five times the case counts compared to a model that is 30× larger. Our method forecasts unseen lineages months in advance.

  Available since 2024.

  Download: https://github.com/UIUC-ChenLab/PandoGen

- **New! ISDC:** ISDC is a novel feedback-guided iterative system of difference constraints (SDC) scheduling algorithm for high-level synthesis (HLS). ISDC leverages subgraph extraction-based low-level feedback from downstream tools like logic synthesizers to iteratively refine HLS scheduling. Technical innovations include: (1) An enhanced SDC formulation that effectively integrates low-level feedback into the linear-programming (LP) problem; (2) A fanout and window-based subgraph extraction mechanism driving the feedback cycle; (3) A no-human-in-loop ISDC flow compatible with a wide range of downstream tools and process design kits (PDKs). Evaluation shows that ISDC reduces register usage by 28.5% against an industrial-strength open-source HLS tool.

  Available since 2024.

  Download: https://github.com/google/xls