Deming Chen

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Education

B. S. Chemistry	Amoy (Xiamen) University, Xiamen, China, 1990
B. S. Computer Science	University of Pittsburgh, Pittsburgh, 1995
M. S. Computer Science	University of California, Los Angeles, 2001
Ph. D. Computer Science	University of California, Los Angeles, 2005

Current and Previous Academic Positions

Aug. 2015 – present	Professor
Aug. 2011 – 2015	Associate Professor
Aug. 2005 – 2011	Assistant Professor Department of Electrical and Computer Engineering University of Illinois, Urbana-Champaign
Aug. 2015 – present	Affiliate Professor (0%)
Aug. 2011 – 2015	Affiliate Associate Professor (0%)
Aug. 2008 – 2011	Affiliate Assistant Professor (0%) Computer Science Department University of Illinois, Urbana-Champaign

Other Professional Experiences

Jun. 2016 – present	President and Co-founder, Inspirit IoT, Inc. Champaign, Illinois
Mar. 2001 – Jul. 2002	Software Engineer, Aplus Design Technologies, Inc. Los Angeles, California
Jul. 1995 – Sep. 1999	System Engineer, Applied Systems Associates, Inc. Murrysville, Pennsylvania
Sep. 1990 – Sep. 1991	Research Staff, Institute of Coal Chemistry Chinese Academy of Sciences, China

Visiting or Seconded Positions

Jul. 2012 – Sep. 2012	Visiting Associate Professor Center for Energy-Efficient Computing and Applications Peking University, China
Oct. 2012 – Dec. 2012	Visiting Associate Professor Department of Electrical Engineering Stanford University, USA

Mar. 2010 – Present	Seconded faculty appointment Advanced Digital Sciences Center (ADSC), Singapore

Research Summary

Deming Chen has published more than 145 refereed journal and conference papers in the areas of FPGA (synthesis, computing, architecture), EDA (system-level/high-level/logic synthesis), GPU (compilation, computing), nanotechnology (device modeling, nano-circuits, nano-architectures), and heterogeneous computing (application mapping for systems with a mixture of multicore/FPGA/GPU). In the recent years, he is also actively involved with other research directions, such as computational genomics, hardware security, and computation in smart grid. Some of these recent works produced high-impact results as well. For example, he led a group of researchers to develop a new DNA error correction tool, which has been downloaded for more than 2000 times from ~50 countries since January 2014 when the corresponding paper was published in the journal *Bioinformatics*. Another example is the GNRFET (Graphene Nano-Ribbon FET) model developed by his group that has been downloaded for more than 1000 times so far. Also, he has been leading the FCUDA project (the CUDA-to-FPGA compiler) since 2008. This package is open source now to benefit both the industrial and academic researchers. He has served as PI/Co-PI on more than 25 research grants administered by US Federal agencies as well as the industry with a total amount of $4.8M to support his research. In addition, he has been a seconded faculty member for the Illinois ADSC center in Singapore since March 2010, supervising a research group there with a total amount of $3.0M. He has received six Best Paper Awards (ASPDAC'09, SASP'09, FCCM'11, SAAHPC'11, CODES+ISSS'13, and ICCAD'15) and numerous other awards. He has served as Associate Editor for several leading journals, and General Chair, Program Chair, Track/Subcommittee Chair, or TPC member for many important conferences in his research areas. He was involved in two startup companies. He implemented his published algorithm on CPLD technology mapping when he was a software engineer in Aplus Design Technologies, Inc. in 2001, and the software was exclusively licensed by Altera and distributed to many customers of Altera worldwide. He is one of the inventors of the xPilot High-level Synthesis package developed at UCLA, which was licensed to AutoESL Design Technologies, Inc. Aplus was acquired by Magma in 2003, and AutoESL was acquired by Xilinx in 2011. He is also an active consultant for several leading semiconductor companies.

Teaching Experiences

- Fall 2003/2004, Teaching Assistant, CS 258G: Logic Synthesis of Digital Systems, University of California, Los Angeles
- Spring 2008/2009/2010, ECE 412: Microcomputer Laboratory
- Spring 2006/2007/2009, Fall/2016, ECE 425: Introduction to VLSI System Design
- Fall 2006/2007, ECE 598BL: Design and Synthesis of System-on-a-chip (new course developed)
- Fall 2008/2009/2010/2011/2013/2015, ECE 527: System-on-Chip Design (permanent version of ECE 598BL above)
- Fall 2011, ECE 411: Computer Organization and Design
- Spring 2012/2013/2016, Fall 2014, ECE 385: Digital Systems Laboratory
- Fall 2013/Spring 2014, ECE 298: Digital System Design Laboratory (new course developed). This course became the new ECE 385 course in Fall 2014, which is a required course for all ECE undergraduate students.

Awards and Honors

- Achievement Award for Excellent Teamwork, Aplus Design Technologies, Inc, 2001

- "Power Modeling and Characteristics of Field Programmable Gate Arrays" – one of the most-downloaded articles from IEEE Transactions on CAD, 2006
- Strathmore's Who's Who, 2007-2008
- Arnold O. Beckman Research Award, UIUC, 2007
- NSF Career Award, 2008
- Included in the List of Teachers Ranked as Excellent, Spring 2008
- Best Paper Award, IEEE/ACM Asia and South Pacific Design Automation Conference, 2009
- Best Paper Award, IEEE Symposium on Application Specific Processors, 2009
- ACM SIGDA Outstanding New Faculty Award, 2010
- Best Paper Award, IEEE International Symposium on Field-Programmable Custom Computing Machines, 2011
- Best Paper Award, Symposium on Application Accelerators in High Performance Computing, 2011
- Senior member of IEEE, 2011
- Best Paper Award Nomination, IEEE International Conference on Field-Programmable Technology, 2011
- Best Paper Award, IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2013
- 10-Year Retrospective Most Influential Paper Award Nomination, IEEE/ACM Asia and South Pacific Design Automation Conference, 2014
- IBM Faculty Award, 2014/2015
- Keynote speech, IEEE International Conference on Anti-counterfeiting, Security, and Identification, 2014
- Distinguished Visiting Professor, 2015-2017, Fudan University, China
- Donald Biggar Willett Faculty Scholar, College of Engineering, University of Illinois, 2015
- Keynote speech, IEEE International Conference on ASIC, 2015
- Best Paper Award, IEEE/ACM International Conference on Computer-Aided Design, 2015
- Distinguished Service Award, ACM, 2016
- Keynote paper, *Integration, the VLSI Journal,* 2016

Research Grants and Contracts

- Research gift, Altera, $20,000, (PI: Chen portion=**$10,000**), 2006
  Title: Novel Logic Synthesis for the New Challenges in FPGAs
- SRC, $360,000, (co-PI, Chen portion=**$180,000**), 2007-2010
  Title: Modeling, Mitigating, and Tolerating Faults due to Parameter Variation in Multicores: A Microarchitecture and CAD Approach
- Research gift, Altera, $15,000, (PI, Chen portion=**$7,500**), 2007
  Title: New Techniques in Synthesis and Physical Design for FPGAs
- NSF, $1,386,000, (co-PI, Chen portion=**$442,000**), 2007-2011
  Title: High-performance Reliable Computing: Addressing the Parameter-variation Challenge through a Cross-disciplinary Architecture, CAD, and Compiler Approach
- NSF, **$400,000**, CAREER Grant, Single PI, 2008-2013
  Title: CAREER: Nano-Centric Design Methodology for Nanoscale FPGAs
- Research gift, UIUC research board, $12,000, (co-PI, Chen portion=**$6,000**), 2008
  Title: SOS: A Nanotube-Based Configurable Logic Fabric
- Research gift, Altera, $20,000, (PI, Chen portion=**$10,000**), 2008
  Title: Novel FPGA Synthesis for Low Power
- Research gift, Sun Microsystems, **$23,000**, Single PI, 2008-2010

Title: Reliable Circuit Design Methodology
- Intel Undergraduate Research Program (ISUR), **$3,200**, Single PI, 2009-2010
- MARCO/DARPA, Gigascale System Research Center, **$236,400**, Single PI, 2009-2012
  Title: Parallel Programming Flow for Efficient FPGA Execution
- Internal gift fund to support PI's research at UIUC, Advanced Digital Sciences Center (ADSC), **$500,000**, Single PI, 2010-2016
  Title: GPU, Reconfigurable Computing, and High-level Synthesis for Application Acceleration
- ADSC/Singapore, **$1.3M**, Grant to support research within ADSC, Single PI, 2010-2013
  Title: Accelerating Immersive Remote Reality Using FPGAs and GPUs
- Research gift, Intel, **$25,000,** Single PI, 2012-2013
  Title: High-Level Synthesis for Accelerator Evaluation and Generation
- UIUC IN^3 (Interdisciplinary Innovation Initiative) fund, Office of the Vice Chancellor for Research/Liberal Arts & Sciences, $200,000, (one of 7 PIs, Chen portion=**$22,000**), 2012-2014
  Title: Developing an Interdisciplinary Research Program in Cancer Genomics
- NSF/SRC, $350,000, (PI, Chen portion = **$175,000**), 2013-2016
  Title: Collaborative Research: From High-level Synthesis to Layout: a Cross-layer Methodology for Large-scale Reliable IC Design
- SRC/DARPA, Center for Future Architectures Research (C_FAR), **$450,000**, Single PI, 2013-2015
  Title: Scalable Synthesis, Exploring Emerging Technologies for Accelerators, and Mapping Diverse Software to Heterogeneous Architectures
- Intel, **$300,000**, Single PI, 2013-2016
  Title: Customized Polyhedral Compilation for Low-Power High-Level SoC Synthesis
- ADSC/Singapore, **$1.4M**, Grant to support research within ADSC, PI, 2013-2016
  Title: Next-Generation Compilers and Architectures for Computation Acceleration with Energy Efficiency
- Research gift, IBM, **$75,000**, Faculty Award, 2014, 2015
  Title: DNA Data Error Correction and Compression with IBM Power8 System
- NSF, **$120,000** as the Graduate Research Fellowship given to a graduate student, 2013-2016
  Title: NSF Graduate Research Fellowship for Research on Hardware Security
- NSF, Research Fellowship for a graduate student (equivalent to one RA support), 2014-2015
  Title: CompGen Fellowship for DNA Error Correction and Genome Mapping
- SRC, $390,000, PI (Chen portion=**$165,000**), 2014-2017
  Title: A New Modular and Global High-level Synthesis Engine for Rapid Post-Silicon Validation of Customized Hardware and Accelerators
- NIH, $1,300,000, co-PI, 2015-2018
  Title: Genomic Compression: From Information Theory to Parallel Algorithms
- Research gift, Jump Trading, **$105,000**, PI, 2015-2017
- IBM, C3SR Center, Co-PI, 2016-2019.
- NSF and industrial partners, CCBGM Center, Co-PI, 2016-2019

Hardware Donations

- Equipment grant, Intel, equivalent to $20,000, 2005
- FPGA boards (30 DE2 boards, two DE3 boards, and one DE5 board), Altera, equivalent to $28,000, 2006, 2009, 2013
- TRDB_DC2 1.3Mega Pixel Digital Camera Module (30 items), Altera, equivalent to $2,100, 2006.

- FPGA boards (one Virtex-5 board, 25 Zedboards, and one high-end Virtex-7 board), Xilinx, equivalent to $19,000, 2009, 2013, 2014
- 260 DE2-115 FPGA boards, Altera, equivalent to commercial value of $130,000, to be used in ECE 385, the new course version developed, 2014, 2015, 2016
- Altera Arria 10 board, equivalent to $4000, 2016.

Software Donations and Instruction Grants

- Software donation, Microsoft
- Quartus II design environment and Nios II embedded soft processors (30 licenses), Altera
- Xilinx Vivado Design Suite (50 licenses), Xilinx
- UIUC SIIP (Strategic Instructional Initiatives Program) fund, UIUC College of Engineering, one of 16 PIs, $125,000 for the first year, 2012-2015

Professional Activities, Membership, and Services

Editorship:

- Associate Editor, IEEE Transactions on Circuits and Systems II (TCAS-II), 2016 – present
- Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2013 – present
- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2012 – present
- Associate Editor, IET Cyber-Physical Systems: Theory & Applications, 2016 - present
- Associate Editor, Journal of Low Power Electronics (JOLPE), 2009 – present
- Associate Editor, Journal of Nanotechnology: Nanomedicine & Nanobiotechnology (NTMB), 2014 – present
- Guest Associate Editor, ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2015-2016
- Associate Editor, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2009 – 2015
- Associate Editor, IEEE Transactions on Circuits and Systems I (TCAS-I), 2009 – 2012
- Lead Guest Editor for a special issue of Journal of Electrical and Computer Engineering on "ESL Design Methodology", 2011
- Associate Editor, Journal of Circuits, Systems and Computers (JCSC), 2009 – 2012
- Associate Editor, ACM SIGDA Electronic Newsletter, 2008 – 2010
- Associate Editor, VLSI Circuit and Semiconductor Technology Division, Translated Series on Foreign Advanced Technologies, China Machine Press, 2007

Professional Society Membership and Leadership:

- IEEE, member since 2000; IEEE Circuits and Systems Society
- ACM SIGDA, member since 2003
- Member, The Design Automation Technical Committee (DATC), IEEE Computer Society, 2009 – 2012
- Member, ACM SIGDA FPGA, Configurable Computing Technical Committee, 2010 – present
- Co-chair, ACM SIGDA Logic/RTL Synthesis Technical Committee, 2010 – 2013

Service to Professional Conferences:

Various chair positions

- Session chair, IEEE International Conference on Computer Design (ICCD), 2005, 2010
- Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2007, 2011, 2014
- Session chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2007-2011
- Session chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2008, 2010, 2013, 2014
- Session organizer or chair, IEEE/ACM Design Automation Conference (DAC), 2009, 2010, 2014
- Session chair, Design, Automation and Test in Europe (DATE), 2009
- Session chair, IEEE System Level Interconnect Prediction (SLIP), 2009, 2010
- TPC Subcommittee chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2009, 2010, 2011, 2013
- TPC CAD track co-chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- TPC CAD track chair/co-chair, IEEE International Symposium on Circuits and Systems (ISCAS), 2010-2011
- TPC Track chair, IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2011
- TPC Track chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2012
- TPC Track chair, IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2012
- Finance chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2010
- Publications chair, IEEE Symposium on Application Specific Processors (SASP), 2010
- Finance chair, IEEE Symposium on Application Specific Processors (SASP), 2011
- Program chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2011
- CANDE Workshop chair, 2011
- General chair, IEEE/ACM System Level Interconnect Prediction (SLIP), 2012
- Program chair, Pacific-Rim Outlook Forum on IC Technology (PROFIT), 2012
- Publicity chair, IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2013-2015
- TPC Track chair, IEEE International Conference on Computer Design (ICCD), 2014-2016
- TPC Track chair, IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2014-2016
- Program chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2015
- General chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2016
- Program co-chair, First International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC), 2015
- Finance chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2017
- Program co-chair, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2017

Technical program committee member

- ACM/SIGDA International Symposium on FPGA (FPGA), 2006-2017
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2007-2011, 2013-2014
- IEEE International Symposium on Circuits and Systems (ISCAS), 2007-2008, 2010-2011

- IEEE International Conference on Computer Design (ICCD), 2007-2016
- International Conference on Field Programmable Logic and Applications (FPL), 2008-2017
- IEEE/ACM International Symposium on Quality Electronic Design (ISQED), 2009-2014
- IEEE International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2009-2011
- IEEE Reconfigurable Architectures Workshop (RAW), 2009-2010
- IEEE/ACM Design Automation Conference (DAC), 2009-2011, 2015-17
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- IEEE Symposium on Application Specific Processors (SASP), 2009
- IEEE/ACM System Level Interconnect Prediction (SLIP), 2009-2012
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2009-2012
- International Workshop on High-Performance Reconfigurable Computing Technology and Applications (HPRCTA), 2009-2010
- ACM/SIGDA Ph.D. Forum at DAC, 2007-2014
- IEEE International Conference on VLSI Design (VLSI), 2010-2011
- Design, Automation, and Test in Europe (DATE), 2010-2011
- IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2010-2016
- Workshop on Emerging Parallel Architectures (WEPA), 2011-2012
- International Workshop on Logic and Synthesis (IWLS), 2011
- IEEE International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES), 2013-2014
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2014
- IEEE International Conference on High Performance Computing (HiPC), 2015
- Steering Committee Member, IEEE/ACM System Level Interconnect Prediction (SLIP), 2014-2016

Panel/Special Session/Workshop organizer

- Workshop co-organizer and co-coordinator: “Grand Challenges in FPGA Research”, 2007
- Panel chair and moderator: “CMOS vs. NANO: Comrades or Rivals,” ACM/SIGDA International Symposium on FPGA, 2009
- Panel organizer and moderator, "Impact of Emerging Interconnect Technologies on SLIP Research Directions", IEEE/ACM System Level Interconnect Prediction (SLIP), 2009
- ACM/SIGDA 2009 University Booth Keynote Speech organizer and moderator, 2009
- Hot Topic Session co-organizer, “Memristor: Device, Design and Application”, Design, Automation, and Test in Europe (DATE), 2010
- Special session organizer: IEEE International Symposium on Integrated Circuits (ISIC), 2014
- Special session organizer: IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2013
- Special session organizer: IEEE International Conference on ASIC (ASICON), 2011, 2015
- Special session organizer: IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2016
- Keynote session co-organizer: IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2017

Tutorial, Panelist and Others

- Panelist: “Best ways to Use Billions of Devices on a Chip,” IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2008

- Tutorial presenter: "Latest Advances and Future Opportunities on CAD for FPGAs," IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2008
- Tutorial organizer and presenter: "From Nanodevices to Nanosystems: Promises and Challenges of IC Design with Nanomaterials," IEEE/ACM Design Automation Conference (DAC), 2009
- Session discussion panelist, IEEE/ACM System Level Interconnect Prediction (SLIP), 2009, 2010
- Dragon Star Lecture Series, Sichuan University, China, 2011
- Tutorial organizer and presenter: "The Device-to-System Spectrum – A Tutorial on IC Design with Nanomaterials," Design, Automation & Test in Europe (DATE), 2012
- Short lectures: "SoC Design Methodology," School of Information Science and Technology, Xiamen University, China, 2012
- Tutorial co-organizer and presenter: "High-Level Synthesis for Low-Power Design," IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2014
- Tutorial instructor: "Bloom-filter Based DNA Error Correction and Acceleration Using FPGAs," Workshop on Genome Assembly and Annotation, Bio IT World Conference & Expo, Boston, 2014

Proposal Review

- External proposal reviewer, Natural Sciences and Engineering, Research Council of Canada, 2008, 2009, 2010
- External proposal reviewer, Israel Science Foundation, 2008
- External research proposal reviewer, Qatar National Research Fund, 2009, 2011, 2012, 2014
- External research proposal reviewer, Nanyan Technology University, Singapore, 2010
- NSF panelist, Computing and Communications Foundations Division, 2012
- NSF panelist, Computing and Communications Foundations Division, 2012
- External proposal reviewer, Intramural Discovery Grant Program, Vanderbilt University, 2013
- Proposal reviewer for U. S. Army Research Office, 2014
- NSF panelist, CISE, 2015
- NSF panelist, CISE, 2016

Journal Review

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Advanced Packaging (TAP)
- ACM Transactions on Reconfigurable Technology and Systems (TRETS)
- IEEE Transactions on Nanotechnology (TN)
- Integration, the VLSI Journal
- Journal of Low Power Electronics (JOLPE)
- IET Circuits, Devices & Systems
- IEEE Design & Test of Computers
- IEEE Transactions on Industrial Informatics
- Applied Physics A
- ACM Transactions on Architecture and Code Optimization (TACO)

- IEEE Transactions on Cyber-Physical Systems (TCPS)
- Briefings in Bioinformatics

Student and Research Staff Advising

Current Graduate Students: (Ph.D. Candidate indicates that the student has passed the Ph.D. qualifying exam**)**

- Keith Campbell (Ph.D. Candidate)
- Daniel Chen
- Ashutosh Dhar (Ph.D. Candidate)
- Di He (Ph.D. Candidate)
- Sitao Huang (Ph.D. Candidate)
- Dae Hee Kim
- Choden Konigsmark (Ph.D. Candidate)
- Huiren Li
- Yi Liang (Ph.D. Candidate)
- Chen-Hsuan Lin (Ph.D. Candidate)
- Jong Bin Lim (Ph.D. Candidate)
- Xinheng Liu
- Gowthami Manikandan
- Anand Ramachandran (Ph.D. Candidate)
- Kenny Umenthum
- Zhangqi Xu
- Xiaofan Zhang
- Chuanhao Zhuge
- Wei Zuo (Ph.D. Candidate)

Current Research Group Members within ADSC (Illinois Center in Singapore):

- Tan Nguyen (Software Engineer)
- Liwei Yang (Software Engineer)

Alumni:

- Lei Cheng, Ph.D., 2007 (co-advised with Prof. Martin Wong; joined Synplicity)
- Shoaib Akram, M.S., 2009 (joined Institute of Computer Science, Foundation for Research and Technology, Greece)
- Scott Cromar, M.S., 2009 (joined law school, UIUC)
- Scott Chilstedt, M.S., 2010 (joined IBM)
- Greg Lucas, M.S., 2010 (joined Intel)
- Chi-Chen Peng, M.S., 2010 (joined Springsoft; now Synopsys)
- Chen Dong, Ph.D., 2010 (joined Magma; now Synopsys)
- Artem Rogachev, M.S., 2012 (joined TI)
- Lu Wan, Ph.D., 2012 (joined Tensilica; now Cadence)
- Alex Papakonstantinou, Ph.D., 2012 (joined NVidia)
- Jacob Tolar, M.S., 2013 (joined Yahoo)
- Chong Li, M.S., 2013 (joined University of Washington as a Ph.D. student)
- Amit Sangai, M.S., 2013 (joined low school, India)
- Chunan Wei, M.S., 2014 (joined Qualcomm)

- Ying Chen, M.S., 2015 (joined Google)
- Pranay Vissa, M.S., 2015 (joined a startup)
- Yun Heo, Ph.D., 2015 (joined Samsung)
- Ying-Yu Chen, Ph.D., 2015 (joined Synopsys)
- Warren Kemmerer, M.S., 2016 (joined Intel)
- Yan Yan, M.S., 2016 (joined Google)
- Zelei Sun, M.S., 2016 (joined Google)

- Dr. Eric (Yun) Liang, postdoc researcher (Research Scientist) of ADSC (2010-2012), now assistant professor in CECA center, Peking University, China
- Dr. Gabriel Noaje, postdoc researcher (Research Scientist) of ADSC (2013-2014), now Senior Computational Scientist at A*STAR Computational Resource Centre, Singapore
- Dr. Swathi Gurumani, postdoc researcher (Principal Research Engineer) of ADSC (2012-2016), now VP of Engineering of Inspirit IoT, Inc.
- Dr. Kyle Rupnow (Senior Scientist) of ADSC (2010-2016), now CTO of Inspirit IoT, Inc.

- Undergraduate Researchers: Bryan Clodfelter, Jaeho Lee, Kyungmin Lee, Allyson Moisan, Andrew Ryan, Alexander Uribe, Yohannes Kifle, Christine Lee, Wenxun Huang, Artem Rogachev, Shuotao Xu, Sai Ma, Chunan Wei, Tielong Su, Liana Nicklaus, Daniel Chen, Chuanhao Zhuge, Xinheng Liu, George Li, Huiren Li, Dae Hee Kim, Kenny Umenthum: many of them are either in top graduate schools (such as MIT and UIUC) or in high-tech companies (such as Microsoft and TI).

Research Interests

- System-level and high-level synthesis
- Computational genomics
- GPU optimization and GPU computing
- Reconfigurable computing
- Computation in smart grid
- Hardware security
- Nanotechnology-centric device modeling, circuit design, and architecture exploration

News Articles

ICCAD Best Paper Award
https://www.ece.illinois.edu/newsroom/article/15131

Chen and Li Named 2015 Willett Scholars
http://www.ece.illinois.edu/newsroom/article/11139

Faculty receive IBM recognition, funding for research contributions
http://csl.illinois.edu/news/faculty-receive-ibm-recognition-funding-research-contributions

Researchers Release First SPICE-compatible Compact Models for Graphene-based Digital Circuits
http://csl.illinois.edu/news/researchers-release-first-spice-compatible-compact-models-graphene-based-digital-circuits

High-level Synthesis on Fire: Research Receives Recognition from Academia, Industry
http://www.ece.illinois.edu/mediacenter/article.asp?id=6013

ECE Receives Zedboard Donation for Research, Education
http://www.ece.illinois.edu/mediacenter/article.asp?id=7389

Chen Receives Intel Gift to Study Increasing Computer Performance and Efficiency
http://www.ece.illinois.edu/mediacenter/article.asp?id=1686

ECE Faculty and Students Win IEEE FCCM Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=1270

Chen and Hwu Win IEEE SASP'09 Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=512

Chen Promotes Nanotechnology Research
http://www.ece.illinois.edu/mediacenter/article.asp?id=182

Graduate Students and Professor Team Up to Win Best Paper Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=181

ECE Faculty Receive CAREER Award
http://www.ece.illinois.edu/mediacenter/article.asp?id=176

Illinois Named an OpenSPARC Center of Excellence
http://www.ece.illinois.edu/mediacenter/article.asp?id=366

Publications

Books

[1] N. Jha and D. Chen, editors, *Nanoelectronic Circuit Design*, Springer Publishers. 2011.

Book Chapters

[1] D. Chen, "Chapter 38: Design Automation for Microelectronics," *Handbook of Automation*, Springer Publishers, 2009.

[2] S. Chilstedt, C. Dong, and D. Chen, "Carbon Nanomaterial Transistors and Circuits," *Transistors: Types, Materials, and Applications*, Nova Science Publishers, 2010.

[3] C. Dong, S. Chilstedt, and D. Chen, "FPCNA: a Carbon Nanotube-Based Programmable Architecture," *Nanoelectronic Circuit Design*, Springer Publishers, 2011.

[4] W. Zuo, S. Gurumani, K. Rupnow, and D. Chen, "New Solutions for Cross-Layer System-Level and High-Level Synthesis," *Emerging Technology and Architecture for Big-data Analytics*, Springer Publishers, 2017.

Monographs

[1] D. Chen, J. Cong, and P. Pan, FPGA Design Automation: A Survey, Foundations and Trends in Electronic Design Automation, NOW Publishers, 137 pages, November 2006.

Journal Papers

[1] D. Chen, J. Cong, M. Ercegovac, and Z. Huang, "Performance-Driven Mapping for CPLD Architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 22, No. 10, pp. 1424-1431, October 2003.

[2] F. Li, Y. Lin, L. He, D. Chen, and J. Cong, "Power Modeling and Characteristics of Field Programmable Gate Arrays," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, Issue 11, pp. 1712-1724, November 2005.

[3] D. Chen, J. Cong, and J. Xu, "Optimal Simultaneous Module and Multi-Voltage Assignment for Low-Power," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 11, Issue 2, pp. 362-386, April 2006.

[4] C. Dong, D. Chen, S. Haruehanroengra, and W. Wang, "3-D nFPGA: A Reconfigurable Architecture for 3-D CMOS/Nanomaterial Hybrid Digital Circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 54, Issue 11, pp. 2489-2501, November 2007.

[5] L. Cheng, D. Chen, and D.F. Wong, "A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 13, No. 2, Article 34, pp. 1-15, April 2008.

[6] L. Cheng, D. Chen, and D.F. Wong, "DDBDD: Delay-Driven BDD Synthesis for FPGAs", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 27, No. 7, pp.1203-1213, July 2008.

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[81] W. Zuo, H. Zheng, S. Gurumani, K. Rupnow, and D. Chen, "New Solutions for System-Level and High-Level Synthesis," *Proceedings of IEEE International Symposium on Integrated Circuits*, December 2014. (**Invited**)

[82] C. Wei, A. Dhar, and D. Chen, "A Scalable and High-Density FPGA Architecture with Multi-Level Phase Change Memory," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2015.

[83] A. Ramachandran, Y. Heo, W.M. Hwu, J. Ma, and D. Chen, "FPGA Accelerated DNA Error Correction," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2015.

[84] K. Campbell, D. Lin, S. Mitra, and D. Chen, "Hybrid Quick Error Detection (H-QED): Accelerator Validation and Debug using High-Level Synthesis Principles," *Proceedings of IEEE/ACM Design Automation Conference*, June 2015.

[85] K. Campbell, P. Vissa, D. Z. Pan, and D. Chen, "High-Level Synthesis of Error Detecting Cores through Low-Cost Modulo-3 Shadow Datapaths," *Proceedings of IEEE/ACM Design Automation Conference*, June 2015.

[86] Y.Y. Chen, Z. Sun, and D. Chen "A SPICE Model for Flexible Transition Metal Dichalcogenide Field-Effect Transistors," *Proceedings of IEEE/ACM Design Automation Conference*, June 2015.

[87] C. Zhuge, C.W. Lung, D. Chen, and Y.K. Jan, "Development of the Feedback Controlled Indentation System for Assessing Risk of Pressure Ulcers," *Proceedings of Rehabilitation Engineering and Assistive Technology Society of North America (RESNA) Annual Conference*, June 2015.

[88] Y. Liang, H. Zhu, and D. Chen, "Optimal Blocker Placement for Mitigating the Effects of Geomagnetic Induced Currents Using Branch and Cut Algorithm," *Proceedings of North American Power Symposium (NAPS)*, October 2015

[89] C. H. Lin, S. Roy, C. Y. Wang, D. Z. Pan, and D. Chen, "CSL: Coordinated and Scalable Logic Synthesis Techniques for Effective NBTI Reduction," *Proceedings of IEEE International Conference on Computer Design*, October 2015.

[90] W. Zuo, W. Kemmerer, J. B. Lim, L.-N. Pochet, A. Ayupoy, T. Kim, K. Han, and D. Chen, "A polyhedral-based SystemC modeling and generation framework for effective low-power design space exploration," *Proceedings of IEEE/ACM International Conference* on *Computer-Aided Design,* November 2015. (**Best Paper Award**)

[91] M. Potkonjak, D. Chen, P. Kalla, and S. P. Levitan, "DA Vision 2015: From Here to Eternity," *Proceedings of IEEE/ACM International Conference* on *Computer-Aided Design,* November 2015. (**Invited**)

[92] L. Yang, Y. Chen, W. Zuo, T. Nguyen, S. Gurumani, K. Rupnow, and D. Chen, "System-Level Design Solutions: Enabling the IoT Explosion," *Proceedings of IEEE International Conference on ASIC*, November 2015. (**Invited**)

[93] L. Yang, S. Gurumani, D. Chen, and K. Rupnow, "Behavioral-Level IP Integration in High-Level Synthesis," *Proceedings of International Conference on Field-Programmable Technology,* December 2015.

[94] L. Yang, M. Ikram, S. Gurumani, D. Chen, S. Fahmy, and K. Rupnow, "JIT Trace-based Verification for High-Level Synthesis," *Proceedings of International Conference on Field-Programmable Technology,* December 2015.

[95] Z. Sun, K. Campbell, W. Zuo, K. Rupnow, S. Gurumani, F. Doucet, and D. Chen, "Designing High-Quality Hardware on a Development Effort Budget: A Study of the Current State of High-Level Synthesis"*, Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2016. (**Invited**)

[96] Y-Y Chen, M. Gholipour, and D. Chen, "Flexible Transition Metal Dichalcogenide Field-Effect Transistors: A Circuit-Level Simulation Study of Delay and Power under Bending, Process Variation, and Scaling," *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2016.

[97] T. Nguyen, S. Gurumani, K. Rupnow, and D. Chen, "FCUDA-SoC: Platform Integration for Field-Programmable SoC with the CUDA-to-FPGA Compiler," *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2016.

[98] X. Liu, Y. Chen, T. Nguyen, S. Gurumani, K. Rupnow, and D. Chen, "High Level Synthesis of Complex Applications: An H.264 Video Decoder", *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2016.

[99] M. T. Satria, W. Zheng, S. Gurumani, K. P. Tee, A. Koh, P. Yu, K. Rupnow, and D. Chen, "Real-Time System-Level Implementation of a Telepresence Robot Using an Embedded GPU Platform," *Proceedings of IEEE/ACM Design, Automation & Test in Europe*, March 2016.

[100] L. Yang, S. Gurumani, D. Chen, and K. Rupnow, "AutoSLIDE: Automatic Source-Level Instrumentation and Debugging for HLS," *Proceedings of IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016.

[101] K. Campbell, L. He, L. Yang, S. Gurumani, K. Rupnow, and D. Chen, "Debugging and Verifying SoC Designs through Effective Cross-Layer Hardware-Software Co-simulation," *Proceedings of IEEE/ACM Design Automation Conference*, June 2016.

[102] S. T. C. Konigsmark, D. F. Wong, and D. Chen, "Information Dispersion for Trojan Defense through High-Level Synthesis," *Proceedings of IEEE/ACM Design Automation Conference*, June

2016.

[103] T. Nguyen, Y. Chen, K. Rupnow, S. Gurumani, and D. Chen, "SoC, NoC and Hierarchical Bus Implementations of Applications on FPGAs Using the FCUDA Flow", *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, July 2016. (Invited)

[104] W. Kemmerer, W. Zuo, and D. Chen, "Parallel Code-Specific CPU Simulation with Dynamic Phase Convergence Modeling for HW/SW Co-Design", *Proceedings of IEEE/ACM International Conference* on *Computer-Aided Design,* November 2016.

[105] S. Huang, G. J. Manikandan, A. Ramachandran, K. Rupnow, W.M. Hwu, and D. Chen, "Hardware Acceleration of the Pair-HMM Algorithm for DNA Variant Calling", *Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, February 2017.

Other Workshop Papers, Poster Papers or Online Publications

[1] C. Dong, S. Chilstedt, and D. Chen, "Variation Aware Routing for Three-Dimensional FPGAs," *Workshop on 3D Integration and Interconnect-Centric Architectures*, Feb. 2009. (A later version with the same title appeared in *IEEE Computer Society Annual Symposium on VLSI*, May 2009.)

[2] A. Papakonstantinou, K. Gururaj, J. Stratton, D. Chen, J. Cong, and W.M. Hwu, "High-Performance CUDA Kernel Execution on FPGAs," *International Conference on Supercomputing*, June 2009. (Two-page extended abstract in the proceeding.)

[3] D. Chen, S. Chilstedt, C. Dong, and E. Pop, "What Everyone Needs to Know about Carbon-Based Nanocircuits," *Online Knowledge Center, Topic: Back-End, Sub-topic: New Technologies and Directions, IEEE/ACM Design Automation Conference*, 2010. (**Invited**)

[4] L. Wan and D. Chen, "Circuit Level Dynamic Behavior Analysis through Timed Ternary Decision Diagram," *Proceedings of IEEE/ACM International Workshop on Logic & Synthesis*, June 2010.

[5] K. Rupnow, Y. Liang, D. Min, M. Do and D. Chen, "Mobile 3D Vision - Algorithm and Platform Challenges," *FPL Workshop on Computer Vision on Low-Power Reconfigurable Architectures*, 2011.

[6] Y-Y. Chen, A. Rogachev, A. Sangai, G. Iannaccone, G. Fiori, and D. Chen, "A SPICE-compatible Model of Graphene Nano-Ribbon Field-Effect Transistors", *NSF Workshop on Nano and Micro Manufacturing*, May 2013.

[7] Y-Y Chen, A. Sangai, M. Gholipour, and D. Chen, "Effects of Process Variation on the Circuit-Level Performance of Graphene Nano-Ribbon Field-Effect Transistors," *Workshop on Variability Modeling and Characterization*, Nov. 2013.

[8] D. Chen, J. Cong, S. Gurumani, W.M. Hwu, K. Rupnow, and Z. Zhang, "System Synthesis and Automated Verification: Design Demands for IoT Devices," *Sensors to Cloud Architectures Workshop*, March 2016.

Ph.D. Thesis

- *Design and Synthesis for Low-Power FPGAs*, Computer Science Department, University of California at Los Angeles, 2005. (Ph.D. advisor: Prof. Jason Cong).

Tool Releases

- **GNRFET HSPICE Model**: First parameterized HSPICE transistor compact models of two types of Graphene Nano-Ribbon Field-Effect Transistors, MOS-GNRFET and SB-GNRFET. Available at nanoHUB.org since July 2013. (More than 1000 downloads so far.)

  Download: http://dchen.ece.illinois.edu/tools.html

- **BLESS**: Bloom-filter-based Error Correction Solution for High throughput Sequencing Reads. Currently, the best DNA error correction tool in terms of quality and small memory usage. Available since January 2014. (More than 2000 downloads so far.)

  Download: http://dchen.ece.illinois.edu/tools.html

- **TIGER**: Tiled Iterative Genome Assembler. Significant improvement over state-of-the-art *de novo* genome assemblers. Available since 2013.

  Download: http://impact.crhc.illinois.edu/Tiger/tiger.aspx

- **H.264 HLS Benchmark**: Fully synthesizable H.264 Video Decoder code, which can be synthesized into RTL with high-level synthesis for FPGA implementation and achieve real-time decoding.

  Download: http://dchen.ece.illinois.edu/tools.html

- **TMDFET SPICE Model**: SPICE transistor models of flexible Transition Metal Dichalcogenide Field-Effect Transistors, TMDFET.

  Download: http://dchen.ece.illinois.edu/tools.html

- **FCUDA**: **Open Source.** A system-synthesis compiler to map GPU CUDA code to FPGA. Enable a common frontend language for heterogeneous compute platforms where FPGA and GPU co-exist. Low-power FPGA computing with comparable performance as GPU.

  Download: http://dchen.ece.illinois.edu/tools.html

Patent Applications

- Patent filed from UIUC/Stanford, 2016.
  Title: Fast and High-Coverage Post-Silicon Validation for Complex SoCs with Accelerators.
  Co-inventors: Keith A. Campbell, Hai Lin, Deming Chen, Subhasish Mitra.

University Services

- Elected into the Executive Committee of College of Engineering, 2016-2019
- Area Chair, Computer Engineering, 2015-2017
- Elected into the Senate of University of Illinois, 2013-2016
- Panelist, campus review panel for GYSS travel grant competition, 2015
- Alternate representative of CSL on the College Executive Committee, 2015-2016
- CSL Director Search Committee, 2014
- Chair, CE Lecturer Search Committee, 2014
- Member, EE Lecturer Search Committee, 2014
- ECE Curriculum Committee, 2013-2014
- CSL Policy and Planning Committee, 2008-2009, 2011-2012, 2014-2016
- Computer Engineering Committee, 2008-2015
- Member of Teaching Evaluation and Awards Committee, 2005-2007
- Graduate ECE Seminar Committee, 2006-2007, 2009

- Graduate Committee, 2007-2009, 2011-2012
- Fellowship Committee, 2009-2012
- Colloquium Committee, 2010-2014
- CSL Build-out Committee, 2012
- Ph.D. committees:
  2006: Dr. Smruti Sarangi (CS, UIUC), Dr. Lei Cheng (CS, UIUC)
  2007: Dr. Liang Deng (ECE, UIUC), Dr. Yu Zhong (ECE, UIUC), Mr. Sain-Zee Ueng (ECE, UIUC), Dr. Yidnek Mekonnen (ECE, UIUC), Dr. Radu Teodorescu (CS, UIUC)
  2008: Dr. Zhiguo Qian (ECE, UIUC), Dr. Tomasz Czajkowski (ECE, U. of Toronto), Dr. Brian Greskamp (CS, UIUC), Dr. Rodolfo Pellizoni (CS, UIUC)
  2009: Dr. Chen Dong (ECE, UIUC)
  2010: Dr. Hui Kong (ECE, UIUC), Dr. Tan Yan (ECE, UIUC), Dr. John Kelm (ECE, UIUC), Dr. Lijuan Luo (ECE, UIUC), Dr. Lu Wan (ECE, UIUC), Dr. Yingying Kuai (ECE, UIUC)
  2011: Dr. Alex Papakonstantinou (ECE, UIUC), Dr. Joon Hyung Chung (ECE, UIUC), Dr. Neal Crago (ECE, UIUC), Dr. Hongbo Zhang (ECE, UIUC)
  2012: Dr. Qiang Ma (ECE, UIUC), Dr. John Stratton (ECE, UIUC), Dr. Xiao-Long Wu (ECE, UIUC), Dr. Feng Xiong (ECE, UIUC)
  2013: Dr. Yuelin Du (ECE, UIUC), Dr. Ting Yu (ECE, UIUC), Dr. Soobae Kim (ECE, UIUC)
  2014: Dr. Eric Kim (ECE, UIUC),
  2015: Dr. Rajesh Bhana (ECE, UIUC), Dr. Yun Heo (ECE, UIUC), Dr. Hee-Seok Kim (ECE, UIUC), Dr. Christine Ying-Yu Chen (ECE, UIUC), Dr. Jungwook Choi (ECE, UIUC), Dr. Pei-Ci Wu (ECE, UIUC), Dr. Kuo-Hsuan Meng (ECE, UIUC), Dr. Joe Meng (ECE, UIUC).
  2016: Mr. Chen-Hsuan Lin (ECE, UIUC), Mr. Yi Liang (ECE, UIUC), Mr. Choden Konigsmark (ECE, UIUC), Mr. Siming Guo (ECE, UIUC), Mr. Wonhyeok Jang (ECE, UIUC), Mr. Glenn Ko (CS, UIUC), Mr. Ti Xu (ECE, UIUC), Mr. Keith Campbell (ECE, UIUC), Dr. Maryam Kazerooni (ECE, UIUC), Dr. Haitong Tian (ECE, UIUC), Dr. Jongsok Choi (ECE, U. of Toronto).

Invited Talks

Title	Conference or Seminar	Location	Year
Design and Synthesis for Low-Power FPGAs	Seminar	Altera Corp., San Jose	2005
VLSI design: turning your big ideas into reality	ECE 200: Undergraduate Seminar	UIUC	2006
Technology Mapping Algorithms for Programmable Logic Devices	ECE 500: Graduate Seminar	UIUC	2006
Abstraction beyond RTL for Low-Power	Computer Engineering Seminar	UIUC	2006
Design and Synthesis for Low-Power FPGAs	Seminar	Velogix Inc., San Jose	2006
3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA Architecture	ECE 590B: Electromagnetics, Optics & Remote Sensing Seminar	UIUC	2007
System, Behavioral, and Logic Level Design Automation	Seminar	T.J. Watson Research Center, IBM	2007
3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA	Computer Engineering/Circuits Seminar	UIUC	2007

Architecture			
3D nFPGA: A CMOS/Nanomaterial Hybrid Reconfigurable Architecture	Workshop on SoC Design Methodologies	Seoul National University, Seoul, Korea	2007
Design and Synthesis for Low-Power FPGAs	Seminar	Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China	2007
VEBoC: Variation and Error-Aware Design for Billions of Devices on a Chip	IEEE/ACM Asia and South Pacific Design Automation Conference	Seoul, Korea	2008
New Design Techniques and Architectures for FPGAs	ECE Seminar	University of Toronto, Toronto, Canada	2008
New Design Techniques and Architectures for FPGAs	Seminar	Altera Corp., Toronto	2008
New Design Techniques and Architectures for FPGAs	Seminar	Xilinx Corp., Toronto	2008
EPOS: an Explicitly Parallel Operations System	Workshop of SoC Design Methodologies	National Tsing Hua University, Taiwan	2008
New Synthesis and Architecture Solutions for Reconfigurable ICs	DLP and VLSI/CAD Workshop	National Tsing Hua University, Taiwan	2008
New Synthesis and Architecture Solutions for Reconfigurable ICs	EE Seminar	National Taiwan University, Taiwan	2008
Variation-Aware Chip Design for Reliability and Performance	Seminar	Sun Microsystems, Inc.	2008
Reconfigurable Circuits Design with Nanomaterials	Design, Automation and Test in Europe (DATE)	Nice, France	2009
New Binding Algorithms for Glitch and Inter-transition Power Reduction	ECSI and USB Workshop on High Level Synthesis: Next Step to Efficient ESL Design	Yokohama, Japan	2009
Nano 3D FPGAs: Design and CAD	Seminar	T.J. Watson Research Center, IBM	2009
FPCNA: A Field Programmable Carbon Nanotube Array	Global COE Workshop	Wasada University, Japan	2009
Design and CAD for Nanoscale Reconfigurable Logic	EE Seminar	Stanford University	2009
New Design Techniques for Existing and Futuristic FPGAs	EECS Seminar	UC Berkeley	2009
Reconfigurable Computing for High Performance	CS Seminar	National University of Singapore	2010
Reconfigurable Computing for High Performance	CE Seminar	Nanyang Technological University, Singapore	2010
New Design Techniques for Existing and Futuristic FPGAs	CSSI Seminar	Carnegie Mellon University	2010
Challenges and Opportunities of ESL Design Automation	Electronic Design Processes Symposium	Monterey, CA	2010
Compilation and Optimization for High Performance	ECE Seminar	Purdue University	2010
FCUDA: Enabling Efficient Compilation of CUDA Kernels onto FPGAs	Asia South Pacific Design Automation Workshop	Incheon, Korea	2010
Challenges and Opportunities of ESL Design Automation	Electronic Design Processes Symposium	Monterey, CA	2010

FCUDA: Efficient CUDA Kernel Compilation for High-Performance Computing on FPGAs	Seminar	NEC, Tokyo, Japan	2011
3D FPGAs with Nanotechnology	NYU-AD 3D Workshop	Abu Dhabi, United Arab Emirates	2011
Porting Performance across GPUs and FPGAs	Pre-conference Workshop at FCCM	Salt Lake City, Utah	2011
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	GSRC eSeminar		2011
Design and CAD for 3D Reconfigurable Circuits	Symposium on 3D TSV Processes and Design Challenges	Singapore	2011
FCUDA: Porting Performance across GPUs and FPGAs	Web seminar	Intel, Oregon	2011
High Level Synthesis of FPGA and Future Nanoscale FPGA Design	Graduate Seminar, School of Information Science and Technology, Xiamen University	Xiamen, China	2011
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	PIC Seminar, IBM	T.J. Watson Research Center, Yorktown Heights	2011
3D FPGAs with Nanotechnology	Nanoelectronic Devices for Defense & Security Conference	New York	2011
High-level Synthesis for FPGA and Futuristic 3D FPGA Design	Departmental Seminar	National Taiwan University	2011
High-level Synthesis for FPGA and Futuristic 3D FPGA Design	Departmental Seminar	National Tsing Hua University	2011
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	Departmental Seminar	University of Wisconsin at Madison	2012
Porting Performance across GPUs and FPGAs through Multilevel Granularity Parallelism	Departmental Seminar	University of Illinois at Chicago	2012
Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	AMD Research Center, Beijing	2012
Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	Tsinghua University, China	2012
Control Flow Optimization and Joint Optimization of Register Allocation and Thread Structure for GPU Computing	Seminar	Microsoft Research Center, Beijing	2012
Control Flow Optimization for GPU Computing and Other Research	Special CS Seminar	Stanford University	2012

Highlights			
GPU Computing and the CUDA-to-FPGA Compiler	Departmental Seminar	University of California at Riverside	2012
GPU Computing and the CUDA-to-FPGA Compiler	Invited panel presentation	T.J. Watson Research Center, Yorktown Heights	2013
GPU Computing and the CUDA-to-FPGA Compiler	Departmental Seminar	Imperial College, London	2013
Optimizations in GPU: Smart Compilers and Core-level Reconfiguration	ACM/IEEE System Level Interconnect Prediction	Austin, TX	2013
Is Graphene Useful for Digital Circuits?	EDA Workshop	Kyoto, Japan	2013
Graphene Nano-Ribbon Field-Effect Transistors as Future Low-Power Devices	IEEE/ACM International Symposium on Low Power Electronics and Design	Beijing, China	2013
Compiler Optimization for GPU Computing	Departmental Seminar	National Taiwan University, Taiwan	2014
Compiler Optimization for GPU Computing	Special Seminar	National Chiao Tung University, Taiwan	2014
New Solutions for High-level Synthesis	Special Seminar	University of Southern California	2014
New Solutions for System and High-level Synthesis	Special Seminar	Harvard University	2014
New Solutions for High Level Synthesis	eSeminar	C-FAR Research Center	2014
New Solutions for System and High-level Synthesis	CS Seminar	School of Computing, National University of Singapore	2014
New Algorithms for Computation Acceleration for Large-scale Smart Grids	IEEE International Conference on Solid-State and Integrated Circuit Technology	Guilin, China	2014
FCUDA: the CUDA to FPGA Compiler	ICCAD 2014 Workshop: Heterogeneous Computing Platforms (HCP)	San Jose, CA	2014
New Solutions for System-Level and High-Level Synthesis	IEEE International Symposium on Integrated Circuits	Singapore	2014
Reliability, Security, and Design Productivity in the Era of IoT	IEEE International Conference on Anti-counterfeiting, Security, and Identification	Macau, China	2014
Boosting Design Productivity for the Internet of Billons of Things	Advanced Digital Sciences Center	Singapore	2014
Quantifying and Improving the Accuracy of Detecting Genomic Variation	NSF I/UCRC Planning Workshop	Chicago, IL	2015
Boosting Design Productivity for the Internet of Billons of Things	China Semiconductor Technology International Conference (CSTIC)	Shanghai, China	2015

Improving Design Productivity for High-Performance and Energy-Efficient Circuits	Special Seminar	Qualcomm, San Jose	2015
New High-level Synthesis Techniques for High-Performance, Energy-Efficiency, and Reliability	Special Seminar	University of Bologna, Bologna, Italy	2015
High Design Productivity for Reliable and Energy-Efficient Circuits in the Era of Internet of Things	Special Seminar	Fudan University, China	2015
High-Level Synthesis, Computational Genomics and Emerging Technologies	Invited talk in a panel	Zhejiang University, China	2015
High Design Productivity for Reliable and Energy-Efficient Circuits in the Era of Internet of Things	IEEE International Conference on ASIC	Chengdu, China	2015
Designing High-Quality Hardware on a Development Effort Budget: A Study of the Current State of High-Level Synthesis	IEEE/ACM Asia and South Pacific Design Automation Conference	Macau, China	2016
System Design Automation Techniques for FPGAs with High-Performance, Energy-Efficiency, and Reliability	Special Seminar	Toyota, San Jose	2016
Reliable and Energy-Efficient Circuit Design in the Era of Internet of Things	Departmental Seminar	Peking University, China	2016
New Advances on High-Level Synthesis	Departmental Seminar	Tsinghua University, China	2016
The CUDA to FPGA Compiler	ShanghaiTech Workshop on Emerging Devices, Circuits and Systems	Shanghai, China	2016
SoC, NoC and Hierarchical Bus Implementations of Applications on FPGAs Using the FCUDA Flow	IEEE Computer Society Annual Symposium on VLSI	Pittsburgh, USA	2016
System Design Automation Techniques for FPGAs with High-Performance, Energy-Efficiency, and Reliability	Special Seminar	Huawei, China	2016
The CUDA to FPGA Compiler	Workshop on FPGAs for Scientific Simulation and Data Analytics	University of Illinois, USA	2016
Automated System-Level Co-design: Are We Finally Ready?	Future Chip 2016: Challenges and Opportunities of Design Automation in China	Tsinghua University, China	2016